EXHIBIT 4

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Dalal et al.

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(45) **Date of Patent: Feb. 22, 2005**

(54) **METHOD AND APPARATUS FOR HIGH SPEED IC TEST INTERFACE**

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(73) Assignee: **Credence Systems Corporation**, Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 402 days.

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(22) Filed: **Oct. 2, 2000**

(51) **Int. Cl.**[7] **G01R 31/28**
(52) **U.S. Cl.** **714/726**; 714/738
(58) **Field of Search** 714/738, 724, 714/726, 742, 739, 733, 727, 731; 365/230; 370/225

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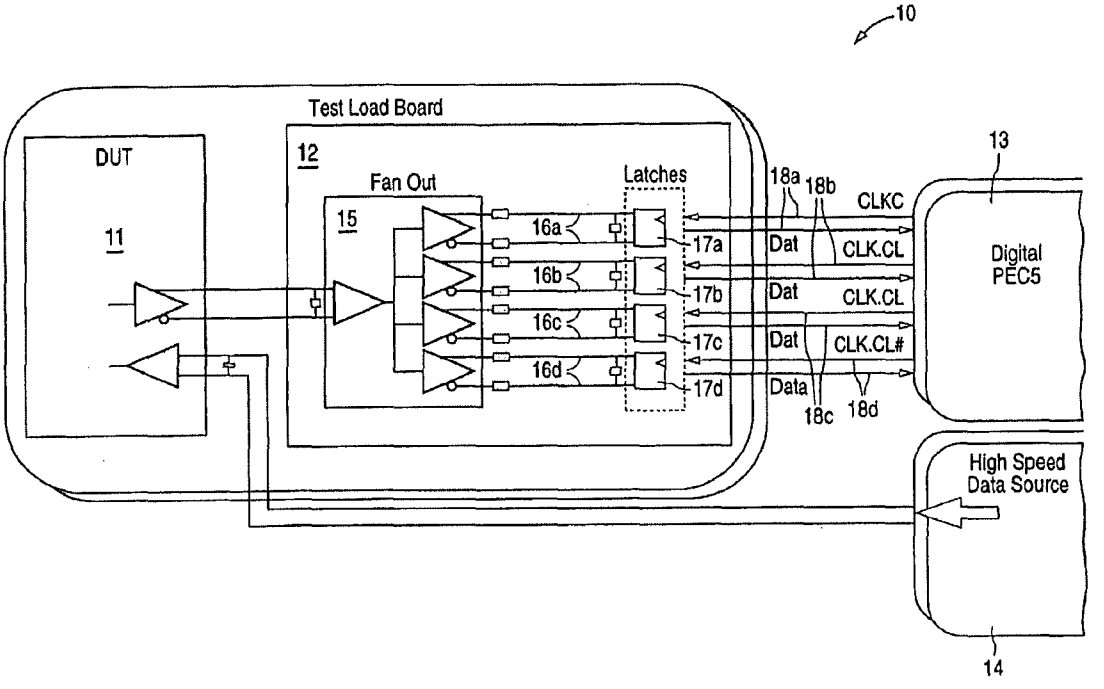
(57) **ABSTRACT**

A testing method and circuit used to test high-speed communication devices on Automatic Test Equipment—ATE. The method and circuit provide a solution to testing very high speed (2.5 Gbps and above) integrated circuits. The circuit fans out the data streams from the output of the Device Under Test (DUT) to multiple tester channels which under-sample the streams. The testing method and circuit also allow for the injection of jitter into to the DUT at the output of the DUT. The skipping of data bits inherent in multi-pass testing is avoided by duplicating the tester resources to achieve effective real-time capture (saving test time and improving Bit Error Rate). Moreover the circuit synchronizes different DUTs with the timing of ATE hardware independent of DUT output data. Also, a calibration method is used compensate for differing trace lengths and propagation delay characteristics of test circuit components.

7 Claims, 4 Drawing Sheets



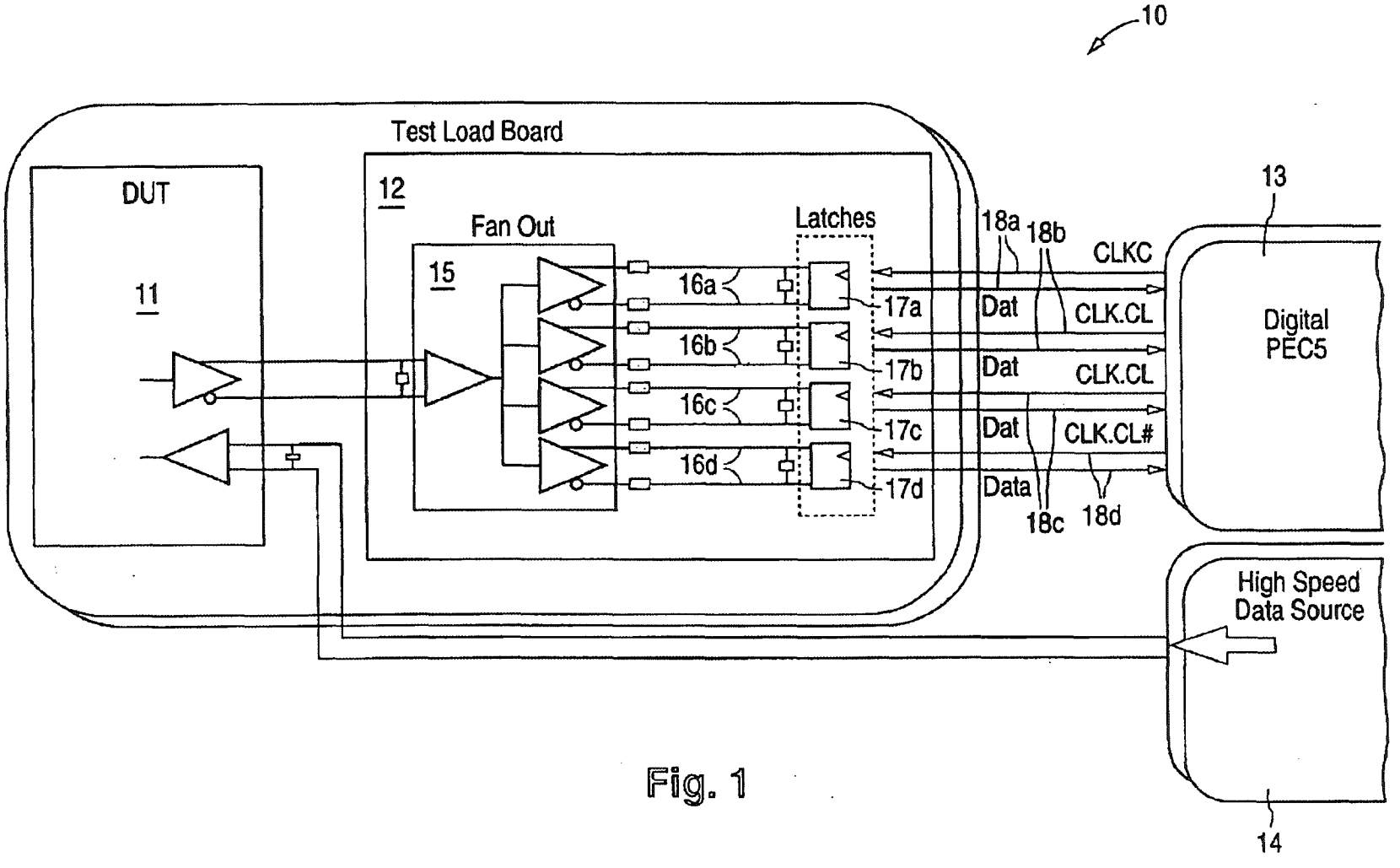

10
Test Load Board
DUT
11
12
Fan Out
15
Latches
16a
16b
16c
16d
17a
17b
17c
17d
18a
18b
18c
18d
CLKC
Dat
CLK.CL
Dat
CLK.CL
Dat
CLK.CL#
Data
13
Digital
PEC5
High Speed
Data Source
14

Fig. 1

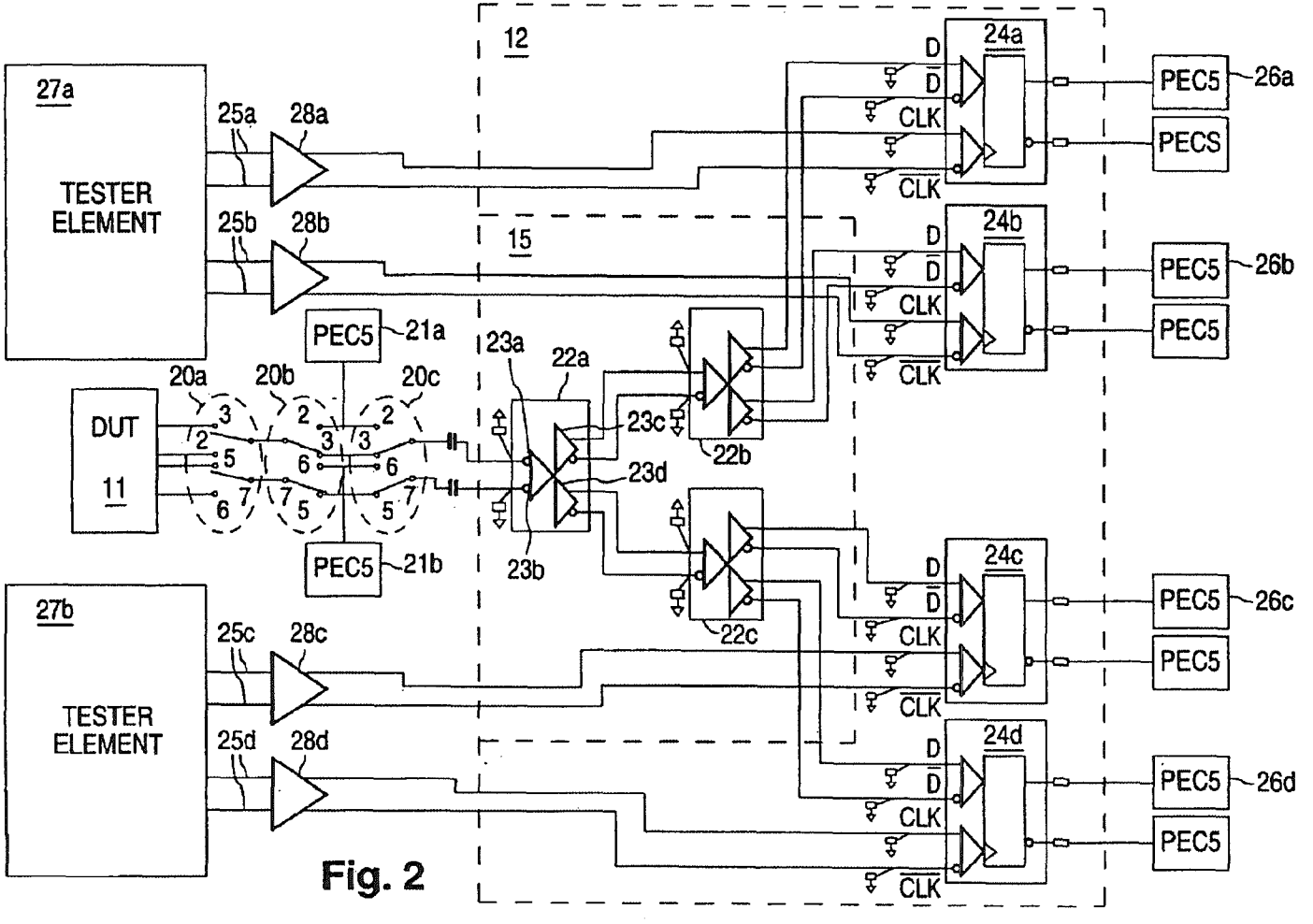

12
15
27a
TESTER ELEMENT
27b
TESTER ELEMENT
DUT
11
25a
28a
25b
28b
25c
28c
25d
28d
PEC5
21a
PEC5
21b
20a
20b
20c
23a
22a
23b
23c
23d
22b
22c
24a
24b
24c
24d
D
D
CLK
CLK
PEC5
PECS
26a
26b
26c
26d

Fig. 2

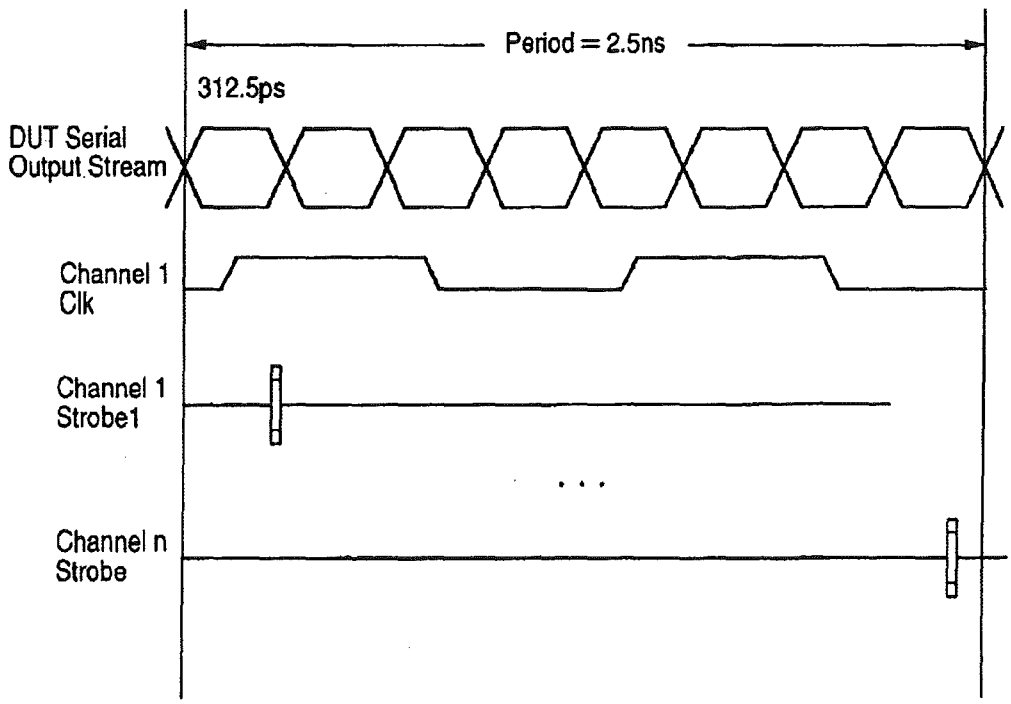

Period = 2.5ns
312.5ps
DUT Serial Output Stream
Channel 1 Clk
Channel 1 Strobe1
Channel n Strobe

Fig. 3

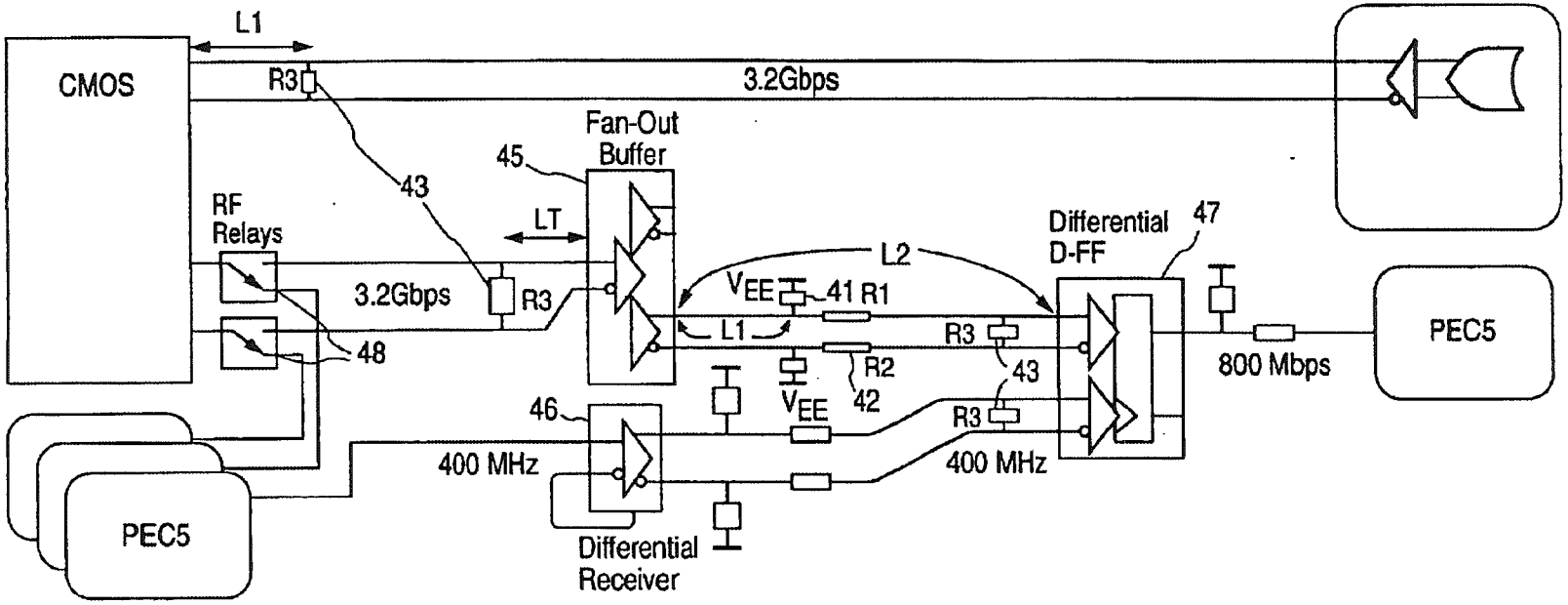

L1
CMOS
R3
3.2Gbps
Fan-Out
Buffer
45
43
LT
RF
Relays
3.2Gbps
R3
48
L2
VEE
41 R1
L1
R2
42
VEE
Differential
D-FF
47
R3
43
R3
800 Mbps
PEC5
46
400 MHz
400 MHz
PEC5
Differential
Receiver

Fig. 4

METHOD AND APPARATUS FOR HIGH SPEED IC TEST INTERFACE

FIELD OF THE INVENTION

This disclosure relates to testing techniques and circuits for testing high-speed communication devices on Automatic Test Equipment (ATE).

RELATED ART

The challenge in testing high-speed electronic circuit interfaces has been present for several years. In most cases in the past the data rates were ten times the standard rate of the available ATE equipment. Some approaches have used multiplexing to provide a high speed data sources to Devices Under Test (DUTs) typically receiving data input at high speeds. See, for example, "Multiplexing Test System Channels for data rates Above 1 Gbps" by David Keezer—Univ. of South Florida, 1990 International Test Conference, Paper 18.3.

Other data handling solutions previously contemplated are tailored toward SONET and Datacom Ics such as that presented in the paper "Frequency enhancement of digital VLSI systems," by Leslie Ackner & Mark Barber—AT&T Bell Labs, Allentown Pa., 1990 International Test Conference, Paper 22.1. At the DUT output where the DUT output signals are tested and compared to expected values, use of a high bandwidth front end latch is introduced. This latch captures the DUT high data rates through multi-pass testing. Multi-pass testing involves sending a particular high-frequency bit stream through test circuitry multiple times and capturing each successive bit during each "pass," or single time that the entire bit stream travels through the circuitry.

In communication devices and applications for high speed networking devices called serializers and de-serializers (SERDES), under-sampling can be harmful in the sense that it masks test failures. A key test is called the Bit Error Rate Test (BERT), referring to the number of bits that are transmitted incorrectly through the communications channel. This BERT number is measured in Parts Per Million (PPM). This number refers to one bit Error for 10^{20} bits transmitted. Under-sampling could potentially mask such errors if it occurs outside of the sampling window. Another technique addresses the problem from the Design-For-Testability standpoint.

Other alternative approaches have been applied to test the DUT. For example, one approach is commonly referred to as the "Loop-back" technique. This method is applicable for SERDES applications. In some electronic devices, a circuit implementing the loop-back is on-chip. This loop-back circuitry connects a serial output pin or port of the device to a serial input pin or port. The advantage of this method is that it is inexpensive and simple to implement. However, there are several disadvantages associated with this method. First, the test data received is restricted to what has been transmitted, which complicates test pattern generation and restricts fault coverage for DUT manufacturing defects. Furthermore, there is no ability to change the input timing. This restricts ability of the testing equipment to characterize the clock recovery mechanism and to inject jitter in order to test the response of the system. The clock recovery mechanism is a mechanism of recovering the clock that is embedded in the data received at the serial input pin or port. Moreover, in non-SERDES applications, a loop-back approach is hard to debug and simulate, as there is no clear

data-in and data-out path. In addition, parametric measurements on the serial input such as Minimum Input Voltage cannot be performed unless the loop is opened, and a direct voltage amplitude control is applied to the serial input. Lastly, output timing parameters of the DUT cannot be tested unless the loop is opened.

Another solution to this problem involves integration of external instruments to expand the bandwidth of the ATE equipment. External instruments can be high bandwidth digitizing scopes, or jitter measurement boxes. The interface may be through a GPIB (General Purpose Interface Bus) protocol. The advantage of using external equipment is the ability to expand the test equipment performance without substantial upgrades. It also allows for a simple correlation between the lab bench characterization environment and the ATE environment. The drawbacks of this method are: (1) it requires a complex interface in order to program GPIB drivers and, (2) the test time is lengthened because the typical GPIB interface is very slow and adds to the testing time substantially. Although the GPIB system drivers are typically available, it takes special effort to perform the link between the ATE software interface and the newly integrated instrument. This may require developing a special graphical user interface (GUI) with special driver commands linking to the scope instrument

SUMMARY

The present disclosure is directed to a testing method and circuits to test high speed communication devices on otherwise conventional (lower speed) Automatic Test Equipment (ATE), e.g., testing very high speed (2.5 Gbps and higher operating speed) integrated circuits operating at speeds higher than conventional testing equipment. The circuit fans out the data stream from the output pins or ports of the Device Under Test (DUT) to multiple ATE tester channels. The testing method and design also allow for the injection of jitter into the output of the DUT for testing purposes. Further, the present invention avoids skipping data bits through multi-pass testing (thus saving test time and Bit Error Rate) by duplicating the tester resources to achieve effective real-time capture. Moreover the present method synchronizes different data communication DUTs to the timing of the ATE hardware. Moreover, there is disclosed a calibration method to compensate for differing trace lengths and propagation delay characteristics of test circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a high-level view of the present test fixture.

FIG. **2** shows a detailed schematic of the tester circuit.

FIG. **3** shows a timing diagram of how tester strobe channels strobe DUT serial output change.

FIG. **4** shows a tester according to one embodiment of the present invention.

DETAILED DESCRIPTION OF INVENTION

FIG. **1** provides a high-level depiction of major components of the present testing system **10**. The data rate of test data from the DUT **11** is several times higher than the base data rate of the conventional portions of test system **10**. An interface circuit **12** is coupled between the DUT **11** and the tester **13** which includes Digital Pin Electronics (PEC) and software operating the system **10**. DUT **11** accepts input from a high speed data source **14**, such as a High Speed Clock Card (HSCC), which can be considered a subcomponent of the tester **13**. Interface circuit **12** branches the

data stream from DUT **11** into multiple tester resources in tester **13**. These tester resources, when used in concert, can accept the very high data rates of interest. Assuming a case of data output at a 3.2 Gbps rate from the DUT **11**, four tester resources (channels) operating at 800 Mbps each would be required to accommodate the DUT rate (4×800 Mbps=3.2 Gbps). System **10** also handles the bandwidth limitation of the tester channels. The high speed DUT **11** output data stream is transmitted through a fan out circuit **15** that replicates the high speed output of the DUT **11** and send the replicated stream along multiple lines **16***a*–**16***d*. Part of each data stream exported from the fan out circuit gets latched through one of several high bandwidth latches **17***a*–**17***d* that is timed differently according to the bit of interest that it is intended to collect from the output of DUT **11**. For instance, in the configuration pictured in FIG. **1**, latch **17***a* collects the first bit output by DUT **11**, latch **17***b* to collects the second bit, latch **17***c* the third bit, and **17***d* the fourth. Effectively, each branch of the fan out circuit **15** is being under-sampled in the time domain (meaning only every n-th bit in the serial data stream is being latched). By controlling the time at which each latch **17***a*–**17***d* is enabled to accept inputs from fan out circuit **15** through latch strobe signals **18***a*–**18***d* (CLK, C) traveling from tester **13** to latches **17***a*–**17***d*, one effectively captures all the data bits of the serial output stream from the DUT **11** in parallel. These bits are captured by Data lines **18***a*–**18***d* traveling from latches **17***a*–**17***d* to tester **13**. (Latch strobe signals, when asserted, enable latches **17***a*–**17***d* to latch onto the value at their respective inputs).

FIG. **2** shows a more detailed version of the structures in FIG. **1**. DUT **11** outputs into a series of relays **20***a*–**20***c* used to connect exclusively the DUT **11**, or calibration pin element (PE) **21***a* and calibration pin element **21***b*, to fan out circuitry **15** in the interface circuit **12**. Fan out buffers **22***a*–**22***c* each accept a single input stream of bits and output two "copies" of those bits. Fan-out buffers **22***b* and **22***c* operate in a manner identical to that of fan-out buffer **22***a*, such that the output sent to each of the four latches **24***a*–**24***d* consists of data streams identical to those inputted into buffer **22***a* The various latches, buffers, etc. of FIG. **2** are conventional so long as they are capable of operating at an adequate data rate.

Each latch **24***a*–**24***d* receives data inputs from the fan-out buffers **22***b* and **22***c* and latch strobe input signals from strobe line pairs **25***a*–**25***d*. The signals transmitted on these signal line pairs are controlled by tester elements **27***a* and **27***d*, which might be High Speed Clock Cards and are part of the tester **13**. Latches **24***a*–**24***d*, when enabled by their respective latch strobe signals from strobe line pairs **25***a*–**25***d*, latch data from their data input pins or ports to their output pins or ports. After a period of propagation delay, this output data is then available for pin elements (PE) **26***a*–**26***d*, which are part of tester **13** in FIG. **1**.

Given that the data rates of many DUTs tested by the system **10** are such that timing errors inherent in the components of system **10** can affect the accuracy of testing results, proper adjustments of the edges of DUT strobes must be assured. This data source is controlled by the tester **13**. A failure to achieve accurate timing would result in incorrect data being captured by the tester **13** including test elements **26***a*–**26***d*. Inaccuracies in timing can result from unmatched trace (conductor) lengths from the tester elements **27***a*–**27***b* to the high speed latches **24***a*–**24***d* that are not compensated for when the latch strobes signals on lines **25***a*–**25***d* are enabled so that latches **24***a*–**24***d* can accept inputs from the DUT **11**. Trace lengths can vary to cause as much as 30 picoseconds variation in propagation delay depending on the location and kind of latches **24***a*–**24***d* used, fan out elements **22***a*–**22***c* that are used, as well as the impedances of the various traces. The traces typically are made as short as possible and are matched in terms of impedances, but mismatches cannot be fully eliminated. Therefore, mismatches must be compensated for. Inaccuracies in timing can also be caused by unequal propagation delays between the fan out IC components **22***a*, **22***b*, **22***c* that are not compensated for, and unmatched timing edge locations among the tester strobe channels.

So that the tester system **10** will strobe latches **24***a*–**24***d* at the proper time in order to avoid the problems mentioned in the previous paragraph, the tester system **10** is calibrated before it is used to test DUTs. The following describes a method to calibrate a testing system using the DUT output to generate a signal resembling a clock signal.

When the calibration process is started, the strobe signal generated by tester element **27***a* travelling on lines **25***a* attached to the first latch **24***a* should enable latch **24***a* to latch the first bit of data from the DUT **11**. (the first latch will latch the first bit of data from the DUT) This is performed by having the DUT **11** transmit a repetitive bit stream, e.g., (1010101 . . .) which simulates a clock signal. Tester **13** searches for the edge transitions (first, second, third transition, etc. . . .) in the repetitive bit stream at the output pin or port of latch **24***a* and determines the time required for the transitions to occur when measured from the start of the calibration process. The proper timing of strobe signals which enable the output signal from latch **24***a*'s output pin or port to be read by the testing equipment, can be determined by software in tester **13** from the measured time of these transitions. The strobe signals traveling on lines **25***a*, which enable a bit transmitted from the DUT **11** to be latched at the input of latch **24***a*, are programmed by software in tester **13** to enable a bit to be latched at fixed time before the strobe produced by tester **13** enables the output signal from latch **24***a*'s output pin or port to be read by the testing equipment **26***a*. (an amount larger than the latch **24***a* propagation delay is sufficient e.g. 500 ps). The strobe signal enabling first latch **24***a* to latch a bit from the output stream of DUT **11** is programmed to latch the first bit, fifth bit, ninth bit, etc. from the output stream of DUT **11** in the circuit depicted in FIG. **2**, because this configuration has four latches **24***a*–**24***d*. However, more or fewer latches could be included in other embodiments

The DUT **11** needs to operate at a sufficiently low speed for calibration such that the data bit width output from the DUT **11** is much longer than the variance in time required for a signal pulse to traverse the various possible paths through the fan-out branches **15**. For data rates of interest, a speed of 400 MHz or less is adequate for the DUT output in this calibration mode (400 MHz is equivalent to 2.5 ns). However, the DUT speed cannot be near DC because the system **10** is designed to test DUTs operating at high frequencies.

This calibration method for the first latch strobe traveling on line pair **25***a* is repeated for the second strobe signal traveling on the second strobe line pair (**25***b*, for example). In this case, the strobe signal enabling the second latch **24***b* to latch bits from the output stream of DUT **11** is programmed to latch the second bit, sixth bit, tenth bit, etc. from the output stream of DUT **11**. The procedure is then applied to all strobe signals for the inputs of the remaining latches. Once this procedure has been performed for all strobe signals transmitted on lines **25***a*–**25***d*, all strobe signals have a phase that is related to the clock phase of the DUT **11**

output at the corresponding latch input location that they strobe. Since the data rate is slow enough, the chance for data bit mixture between the fan-out branches does not exist. The timing of each strobe signal traveling on lines **25***a*–**25***d* needs to be adjusted to the center between edge transitions at the latch inputs. Once the speed of the DUT **11** is changed to its normal operating speed, the strobe timing is normalized by the software in tester **13** to meet the criteria of the preceding sentence for the (typically, higher) speed.

Another relevant calibration method uses calibration PEs **21***a* and **21***b* to calibrate the test system **10**, instead of a DUT **11** which outputs a repeating bit pattern. Calibration elements **21***a* and **21***b* can simulate the repeating bit pattern output by the DUT **11** when used for calibration purposes.

The present disclosure also includes a synchronization technique. One assumption made in using this technique is that the DUT **11** data output phase delay is repeatable. This means that data transitions always occur at the same time relative to the DUT **11** input signal timing. The data content may not be repeatable, but its timing must be. Another way of describing this repeatability is to say that when the DUT **11** is initialized by the tester **13**, the delay between the instant of initialization and when the DUT output clock signal makes its first transition is the same every time a particular DUT **11** is initialized. In the case in which the data output from the DUT **11** is repeatable, no post processing of captured data is required for testing purposes. With a repeatable data output stream, captured data can be compared against expected data for testing purposes.

Synchonization is performed by applying strobe signals to a latch such as **24***a* in the testing circuit at very rapid increments, while the input data at the latch **24***a* is monitored. The time between initialization of the DUT **11** and when the latch **24***a* experiences its first transition at their inputs is determined. The time is measured from the instant of initialization to the time at which the first transition at the input reaches 50 percent of its maximum value. This time corresponds to the time required for the latch **24***a* to begin its first transition at its output pins or ports. Algorithms in the tester **13** determine the clock frequency of an arbitrary DUT **11** that is initialized using this method by using the two timing factors just described In this manner, strobe signals are transmitted allowing the tester **13** to accept DUT **11** output signals from latches **24***a*–**24***d* just when outputs from the latches **24***a*–**24***d* are stable and midway between unstable transition periods. Moreover, the synchronization process just described must only be performed for one latch (such as **24***a*) in order for the timing of strobes for all latch outputs to be determined. The calibration method described above using software in the tester **13** determines propagation delay data for each latch **24***a*–**24***d* relative to one another, and this data can be used to extrapolate proper strobe times for all latch outputs once the strobe time for one latch **24***a* is determined. Further, strobes signals for the respective latch **24***a*–**24***d* outputs are enabled such that successive bits or pulses from the DUT **11** are sent to successive tester data channels **26***a*–**26***d*, this is illustrated in FIG. **3**.

The tester **13** is programmed to strobe output from the latches **24***a*–**24***d* into the tester data channels **26***a*–**26***d* at the proper time location set by the synchronization process. The data expected at each tester data channel **26***a*–**26***d* is a fraction of the original data stream expected from the DUT output. FIG. **3** shows the individual channel timing and expected data.

As mentioned above, one particular implementation uses high speed networking devices called serializers and de-serializer (SERDES). In one implementation, the components illustrated in FIG. **4** are used. These component values with corresponding drawing reference numbers, are shown below:

Resistors:

R1=330 Ohm (**41**)

R2=43 Ohm (**42**)

R3=100 Ohm (**43**)

Fan Out Buffer: part no. MC10EP11 (**45**)

Differential Receiver: part no MC10EL16 (**46**)

High Speed Diff D-FF: part no. MC10EL52 (**47**)

RF Relays: part no. Teladyne RF103 (**48**)

The circuit shown in FIG. **4** also uses the ITS9000KX class of tester from Schlumberger.

The circuit components listed above were chosen to address the following:

1. Test Board traces layout to maintain 50 Ohm environment at multi-giga hertz BW.
2. Maintaining matched trace length for different data/clock pairs.
3. Use proper ECL components that will achieve the speeds required.
4. Level adjustment of the ECL circuit to work with a CMOS part and tester channels
5. Working with differential signals in a single-ended test environment. This was addressed by using special converters.

The circuit parameters above are merely illustrative and other parameters can be chosen to implement the DUT output fan out, calibration, and synchronization methods of the present invention.

The disclosure is illustrative and not limiting; further modifications will be apparent to one skilled in the art in light of this disclosure, and are intended to fall within the scope of the appended claims.

What is claimed is:

1. Apparatus for testing an integrated circuit, comprising:

a data source coupled to the integrated circuit to provide test signals to the integrated circuit;

a plurality of relays selectively coupling the integrated circuit to the apparatus wherein the integrated circuit is tested;

a plurality of fan out elements coupled to receive data pulses from the plurality of relays and to distribute the data pulses to a plurality of latches; and

a strobe element associated with each of the plurality of latches for enabling each of the plurality of latches to transfer the data pulses from an input port to an output port of each lath of the plurality of latches.

2. The apparatus of claim **1**, further comprising testing components of said apparatus each coupled to the receive the data pulses from one of the plurality of latches, the testing components of said apparatus receiving the data pulses at a frequency that is a fraction of the output signal frequency of the integrated circuit being tested.

3. The circuit network of claim **2**, wherein the fraction is equal to the output frequency of the integrated circuit being tested divided by the number of the latches.

4. A method of testing an integrated circuit comprising the acts of:

providing an integrated circuit;

applying signals to an input port of the integrated circuit;

fanning out data pulses received from an output port of the integrated circuit;

distributing each of the data pulses to one of a plurality of latches; and

calibrating a time at which each one of the plurality of latches is enabled by a strobe element.

5. The method of claim **4**, further comprising the acts of:

measuring the time between initialization of the integrated circuit and detection of a first data pulse at an input port of a selected one of the plurality of latches;

calculating a clock frequency of the integrated circuit therefrom, and;

testing the integrated circuit after the measuring and calculating are performed.

6. The method of claim **4**, further comprising the act of transmitting a repetitive bit stream with alternating voltage levels from the integrated circuit to calibrate a time at which each one of the plurality of latches is enabled.

7. The method of claim **4**, further comprising the act of edge transitions at the output terminal of each one of the plurality of latches thereby to calibrate a time at which each one of the plurality of latches is enabled.

* * * * *

EXHIBIT 5

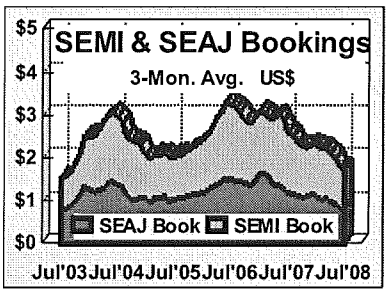
Semiconductor Test DFT News Trends Technology Commentary

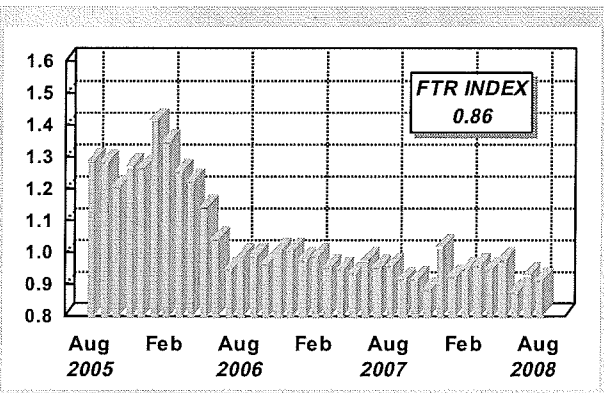
FTR THE FINAL TEST REPORT

Vol. 19 No. 09 September 2008

Slower Orders Finally Result in Weaker Chip Eqpt. Sales

The chipmakers' pullback in capital investments has slowed orders for the better part of a year and has now caught up with the sales side of the equation. The latest monthly data from SEMI shows declines in both bookings and billings that haven't been seen since the last cyclical slump in 2003 and approaching those of some months of the industry's 2001 dark age. Bookings in July reported by North America-based chip equipment makers fell below the $1B mark to $904.8M. That's 3.1 percent lower than June's downwardly revised number and nearly 36 percent lower than a year ago. Billings were down 6.2 percent MoM and down 35.5 percent YoY to $1087.4B, for a book-to-bill of 0.83.





***FTR*'s index of ATE, chipmakers, and PC makers vs. the Dow-30, slipped during August as investors again worried about chip-related shares.**

How bad have booking and billings numbers become for U.S. chip equipment makers? A few benchmarks:

- Bookings were at the lowest level since October '03, the fourth straight month of the >30 percent YoY slump, tying a low-water mark from mid-2005.
- The last time bookings were below the $1B mark was Spring of 2005 (for two months); if it happened again in August that will be a 3-month trend not seen since late 2003.
- We're now at 14 straight months of YoY order declines (49 percent off the peak of $1782.3M two summers ago), a string last seen in 2001-2002.
- Billings are at their lowest since August 2005; the past two months together have seen ~35 percent YoY declines, something the industry hasn't seen since way back in the Spring of 2002.

Continued on page 2

iNSIDE iNFO

 Editor: J. Mulady
THE FINAL TEST REPORT is published by IKONIX Corporation, P.O. Box 1938, Lafayette, CA 94549 USA. Tel:925-939-7909 Fax: 925-906-9427 e:mail: ftr@ikonix.com. Subscription rates and a sample issue are available upon request.

Continued from page 1

Things were no better for Japan's chip equipment makers. Japan's chip equipment book-to-bill finally reached above parity at 1.09 - for the first time in thirteen months - but only because the long string of falling bookings finally resulted in billings falling to ¥84,718 million (US$799.88 million), down 4.0 percent from the June 2008 level of ¥88,283 million and down 49.1 percent from the July 2007 billings of ¥166,458 million.

While the above numbers generally reflect the status of wafer fabrication equipment - and the relatively long times (six to nine months or more) from order receipt to delivery, installation, acceptance and finally billing. Test, assembly and packaging (TAP) orders and billings are an entirely different case. TAP vendors, partially as a result of their outsourcing most or all of their product manufacturing, are able to deliver even their most complex systems in 45 to 60 days after the order is received. Thus 'turns business' (products delivered/billed in the same quarter as the order is received) has become the norm.

This is reflected in the fact that over the first seven months of 2008 SEMI's TAP book to bill was just above unity in three of those months and slightly below unity in the other four. In comparison, SEMI's total equipment B/B never came close to unity in any month this year.

SEMI said that No. American TAP equipment bookings were $196.3 million in July, down 14.2 percent sequentially and 27.8 percent YoY. July billings were almost identical, at $197.9. July TAP billings were $197.9 million, down 7.4 percent sequentially and down 23.8 percent YoY.

Japan-based TAP equipment makers' June 2008 bookings were ¥18.347 million (US$175.61 million), down 6.9 percent MoM, and down 34.6 percent YoY. June billings were ¥19,336 million (US$185.1 million), down 14.2 percent MoM and down 8.6 percent YoY.

While many observers, based on recent chip forecasts, don't expect a major recovery for chip sales anytime soon, Gartner expressed 'surprise' at the semiconductor market's robust 1H'08. It noted that recently released WSTS figures for June, put total semiconductor sales at $25.5 billion, up 26 percent from $20.5 billion in May and up 12 percent from $22.7 billion in June 2007. The June WSTS figure was slightly higher than Gartner's expectation of $25 billion and contributed to Q2 sales of $64.7 billion, up 3 percent sequentially. When combined with Q1 sales of $62.8 billion, total sales in the first half of 2008 were $127.5 billion, a growth of 5 percent compared to the same period in 2007, Gartner noted.

Nevertheless, it continued to warn of a "coming widespread slowdown in the electronics sector. Gartner noted that much of the 5 percent first-half semiconductor sales growth was due to demand from PCs and cell phones, and questioned just how long that will last. Its caution was bolstered to some extent late last month when Dell Computer posted a surprisingly steep drop in quarterly earnings and said companies around the world are cutting back on technology spending - noting particularly about weaker spending in Asia and Western Europe. Dell's profit fell 17 percent YoY for its second quarter ended August 1, to $616 million, or $0.31/share, from the restated year-ago net of $746 million, or $0.33/share. Its revenue however rose 11 percent to $16.43 billion.

"We find it surprising that the chip market has remained remarkably robust in the first half of 2008," Richard Gordon, a research VP at Gartner, said. "The global macroeconomic environment continues to worsen. The effect of the 'credit crunch' on the U.S. (and to some extent European) housing markets) has further eroded consumer confidence. In addition to downbeat sentiment on how well off consumers are feeling, high energy prices are having a material effect on disposable income."

(However, its worth noting that amid all of the widely publicized concern about the U.S. economy - and on-going arguments that this country is "already in recession"- the U.S. Commerce Department on August 28 said that "strong exports and consumer spending supported by government stimulus checks drove the U.S. economy up at a solid 3.3 percent annual rate in the second quarter, much faster than the 1.9 percent rate it had reported earlier.)

In an effort to explain why semiconductor sales have held up well so far this year we need only look at the markets for PCs and cell phones, which dominate semiconductor consumption and have recorded strong unit sales in Q1 and Q2. Notably, it is demand in the emerging regions that has fueled this unit growth in these two important markets.

Gartner projected sales of about $140 billion for the second half, which would represent growth of around 3 percent compared to the same period last year and would lead to annual sales of about $267 billion for an annual growth rate of about 4 percent for 2008 as a whole.

SEMI, in a report released last month, agrees with the general expectation that spending on chip equipment will decline by about 20 percent this year. But, it expects a rebound of more than 20 percent next year - driven by more than 70 fab projects. It said that overall annual fab capacity this year is expected to be about 16 million wafers, up just 9 percent from the 17 percent growth in 2007 - but grow by about 10 percent next year.

With both bookings and sales now slumping in sync, the obvious question is when can we expect them to hit bottom and bounce (particularly on the bookings side)? Dan Tracy, SEMI's senior director of industry research and statistics said: "While chipmakers remain attentive to cost controls, this remains a highly cyclic industry. Factory utilization levels, unit demand growth, and planned fab projects suggest that new investment activity will resume in 2009."

IN FTR'S OPINION

Be careful what you wish for, you just might get it!

Industry pundits have long been calling for consolidation of the players in the ATE industry. Over the past ten months or so they have seen a number of acquisition of chip test related companies. Among them were the acquisition of Applied Precision's semiconductor business by Rudolph Technology for an undisclosed amount of cash and stock: ASSET InterTech acquisition of ITT [financial details were not disclosed as both are privately-held companies] and Verigy's acquisition of Inovys for what the companies said was "not material."

The largest recent acquisition, in terms of cost to the acquirer, was Teradyne's acquisition of Nextest for abut $325 million. Those same pundits complained that Teradyne overpayed for that company. Arguably, to date they were correct - but the final evaluation of that acquisition will have to wait a couple of more years.

However, they are going to be hard pressed to say that about the latest industry consolidation. On August 29th LTX announced the completion of its "merger with" or "acquisition of" (readers choice) of Credence Systems, resulting in the formation of LTX-Credence Corporation in a tax free, all-stock "merger of equals" following the approval of both companies' stockholders.

Under the terms of the merger agreement, Credence stockholders received 0.6129 shares of LTX-Credence stock for each share of Credence stock they own, causing the former stockholders of Credence to hold 50.02 percent of the outstanding shares of the combined company and pre-merger LTX stockholders to hold 49.98 percent of the shares of the combined company.

As of August 29th Credence shares were no longer traded on the Nasdaq. The new company, LTX-Credence, headquartered in Milpitas, CA, will trade on the NASDAQ Global Market under the new symbol *LTXC*, beginning on September 2, 2008.

However, for Credence shareholders it did not end exactly as was hoped when it was announced on June 22. On the last trading day before the announcement Credence's shares closed at $1.25/share and LTX shares closed at $2.81. If the merger had closed on that date, Credence shares would have been valued at about $1.72. However on the closing date of August 28, LTX shares had fallen to $1.96, valuing Credence shares valued at just $1.20, and the company was effectively sold to LTX for about $122 million - a major discount from Credence's market cap of about $4 million on the same date last year. (Note: LTX shares fell $0,17, or 8.7 percent, to close at $1.79 on the day following the merger close.

Dave Tacelli, CEO/president of LTX-Credence, commented: "We have worked diligently to close this transaction, and have successfully completed the merger ahead of schedule. Now, with our seasoned leadership team in place, we will push forward with that same intensity as we move through the integration process and drive to rapidly deliver the advantages of the new LTX-Credence to our stockholders, our customers and our employees."

LTX-Credence will provide an update on the progress of the company's integration activities during a conference call the first full week of October 2008.

Clearly, this oft described as a 'garage sale' of Credence Systems was, in the main, the end-result of its acquisition if NPTest in May 2004 for $660 million in cash and stock and tens of millions of dollars more to close operations and restructure during the digestion process.

Credence was never able to take any real advantage from its acquisition of NPTest - under the management of three different CEO's in the intervening period, each of whom have or will exit the company with substantial amounts of investor cash.

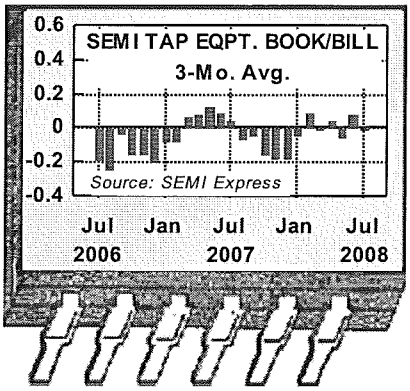
The centerpiece of that acquisition was Credence's 'Open-Architecture' Sapphire SoC tester that was already established as AMD's major tester. However, Credence was never able to succeed with that tester in any quantity at other chipmakers with the exception of STMicroelectronics. As a result the OSATs had no interest in it either. (The one exception being Amkor that reportedly purchased a number of Sapphire systems on AMD's promise to keep them fully utilized with its wafers, but eventually forced AMD to buy them after it failed to do so and Amkor was unable to find any other chipmaker willing to use them.)

Now, AMD is expected to spin-off its manufacturing operations into a new company - likely headed by Hector Ruiz, its executive chairman - reportedly to be partially funded by government-backed Mubadala Development Co. in the UAE capital of Abu Dhabi. That group had already taken an 8 percent equity position in AMD with an investment of $600 million in November 2007.

According to reports from various industry sources to *FTR*, it's likely that the approximately 200 Sapphires - mostly installed in Austin TX and Dresden, Germany, will be moved to wafer probe and replaced at Final Test by Advantest T2000 testers. It's also likely to add some number more systems to its installed base of Verigy 93000 SoC testers for engineering and device characterization.

FTR admits that some of above is speculation on its and others part.

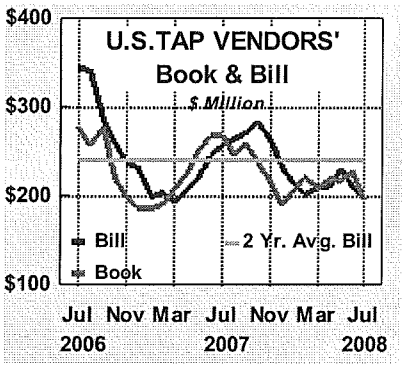
But, that's my opinion.



SEMI's July TAP Eqpt B/B at 0.99

SEMI said that No. American chip equipment vendors reported $904.8 million in bookings (3-month average) in July, down 3 percent sequentially and down 35.7 percent YOY. Total equipment billings were $1,087.4 million in July, down 6.2 percent sequentially and down 35.5 percent YoY, for a B/B of 0.83.

Front-end equipment bookings were $708.5 million in July about flat sequentially and down 37.7 percent YoY. July billings were $889.5 million, down 6.2 percent sequentially and down 37.7 percent YoY, resulting in a book-to-bill ratio of 0.80.

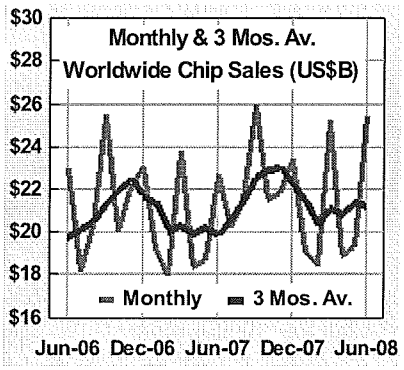


Test, assembly and packaging (TAP) equipment bookings were $196.3 million in July, down 14.2 percent sequentially and 27.8 percent YoY. July TAP equipment billings were $197.9 million, down 7.4 percent sequentially and down 23.8 percent YoY. The TAP equipment book-to-bill for July was 0.99.

The recent very flat book-to-bill ratio for TAP equipment (Graph above) indicates just how dependant it has become on 'turns' business.

TAP Book-to-Bill

	Jun'08	Jul'08	Jul'07
Book	$228.9	$196.3	269.2
Bill	$211.6	$197.9	257.0
B/B	1.08	0.99	1.05



Actual June Chip Sales up 12.2% YoY

The WSTS reported that the global chip market was up 12.2 percent YoY at $25.52 billion in June 2008. The actual data in June compares with an actual market size of $20.25 billion in May 2008, and is evidence of a gathering pace of market growth in 2008, despite concerns over the general economy. Total chip sales were up 4.7 percent in the first half of 2008 to $126.62 billion

However, at the same time the WSTS' latest report indicates that it had reduced total chip revenue data for the first five months of the year by nearly $1.5B or about 1.4 percent. It did not comment on this change The SIA frequently adjusts data through the year. Specifically, the reductions were apparently restricted mostly to MOS Standard Cell and FPLD.s.

Memory pricing continued to drag down the overall chip market. Total IC revenue growth through the first six months of 2008 is a moderate 4.9 percent, But, when memory sales are included. However, if the memory market is excluded, the balance of the IC market is growing at a robust 11.5 percent year-to-date.

June 2008 WW Chip Sales

The SIA said global chip sales for the first half of 2008 grew to $127.5 billion, an increase of 5.4 percent YoY in the first half of 2007. Second-quarter sales were $64.7 billion Up 3 percent sequentially. June sales (3-month avg.) of $21.6 billion were up by 8 percent YoY and up 0.5 percent sequentially. "Continuing strength in international markets - coupled with healthy demand in the U.S. - helped drive higher worldwide sales of semiconductors in June," said SIA president George Scalise. "Key chip demand drivers - especially personal computers, which account for 40 percent of semiconductor sales, and mobile phones, which drive about 20 percent of demand - continued to show double-digit unit growth. JPMorgan recently revised upward its forecast for unit sales of personal computers to 13 percent, with sharp increases in sales of portable systems. Forecasts for unit sales growth of mobile handsets range from 10 to 12 percent for 2008," he added.

(US$Billion)	MoM			YoY	
Market	May'08	Jun'08	%Chg	Jun'07	%Chg
Americas	3.38	3.40	0.7%	3.31	2.8%
Europe	3.33	3.37	1.2%	3.21	5.1%
Japan	4.24	3.95	-6.8%	3.84	2.8%
Asia Pacific	10.52	10.85	3.1%	9.61	12.9%
Total	21.46	21.57	0.5%	19.97	0.8%

June '08 Regional Chip Sales
(US$Billion)

Market	Sales	MoM	YoY
Americas	$4.06	49.6%	11.3%
Europe	$3.99	36.0%	7.4%
Japan	$4.28	15.3%	3.0%
ROA	$13.19	31.9%	17.6%
TOTAL	$25.52	31.8%	12.2%

ATE STOCKS

Ticker	Close 08/29	Change Month	52 Week High	52 Week Low
AEHR	$4.37	-8.8%	$11.20	$4.28
ATRM	$3.75	7.8%	$6.24	$2.60
ATE	$20.91	2.5%	$37.37	$19.31
CSCD	$5.93	3.1%	$10.87	$5.31
COHU	$16.70	4.9%	$22.31	$13.27
CMOS	$1.13	-11.7%	$3.43	$1.00
EGLS	$1.50	0.0%	$2.70	$1.12
EGLT	$14.18	14.4%	$15.00	$9.31
ESIO	$14.29	-8.6%	$25.64	$13.61
FORM	$19.19	10.3%	$48.48	$15.56
INTT	$1.21	-24.4%	$3.39	$1.20
KLIC	$5.14	-19.2%	$9.36	$4.55
LTXX	$1.79	-17.9%	$4.16	$1.79
PHTN	$15.22	2.1%	$15.28	$7.71
TER	$9.33	-0.4%	$15.05	$8.75
VRGY	$18.47	-16.9%	$27.96	$17.04
Avg. Change		**-3.9%**		

1H08 Top 20 Chip Supplier Rankings

IC Insights' recent report uncovered a shake-up in the 1H'08 top 20 chip supplier rankings. There are eight U.S. companies in the top 20 (including three fabless companies), six Japanese, three European, two South Korean, and one Taiwanese company (IC foundry supplier TSMC) in the rankings. As shown below, it required at least $2.1 billion in 1H'08 sales to make the top 20 ranking.

Although the top four companies remained the same, there were a number of "movers and shakers" up and down the remainder of the 1H08 rankings as compared to their 1H'07 positions. Qualcomm and Broadcom made biggest leaps. NXP, and AMD registered the biggest falls.

1H'08 Top 20 Chipmakers by Sales - US$M

Rank 1H08	Rank 1H07	Company	Headquarters	Sales 1H08	Sales 1H07	Yoy % Chg.
1	1	Intel	U.S.	17,496	15,988	9%
3	3	Texas Inst.	U.S.	6,366	6,372	-0%
10	14	Qualcomm	U.S.	3,382	2,626	29%
13	13	Micron	U.S.	2,920	2,698	8%
15	11	AMD	U.S.	2,854	2,611	9%
16	16	Freescale	U.S.	2,693	2,605	3%
19	19	Nvidia	U.S.	2,143	1,743	23%
20	23	Broadcom	U.S.	2,139	1,789	20%
Total U.S. Based				**39,993**	**36,432**	**10%**
4	4	Toshiba	Japan	5,844	5,759	1%
7	8	Renesas	Japan	4,337	3,933	10%
9	9	Sony	Japan	3,430	3,289	4%
12	15	NEC	Japan	2,998	2,712	11%
17	17	Fujitsu	Japan	2,334	2,108	11%
18	21	Panasonic	Japan	2,228	1,775	26%
Total Japan Based				**21,171**	**19,576**	**8%**
2	2	Samsung	So. Korea	11,187	9,249	21%
8	7	Hynix	So. Korea	3,499	4,567	-23%
Total So. Korea Based				**14,686**	**13,816**	**6%**
6	5	STMicro	Europe	4,570	4,039	13%
11	12	Infineon	Europe	3,146	2,643	19%
14	10	NXP	Europe	2,888	2,851	1%
Total Europe Based				**10,604**	**9,533**	**11%**
5	6	TSMC	Taiwan	5,661	4,180	35%
Total Taiwan Based				**5,661**	**4,180**	**35%**
Total Top 20				**92,115**	**83,537**	**10%**

Source: Company Reports. IC Insights — August 2008

FINANCIAL REPORTS

Credence Systems Corp.

Q3 Ending : Aug 3 ($000).

	2008	2007
Sales	$62,000	$114,476
Ops. Pft.	na	(457,366)
Net	na	(461,366)
Per Shr.	na	(4.61)

Kulicke & Soffa Industries

FQ2 Ending June 30 : $000

	2008	2007
Sales	$180,119	$168,625
Ops. Pft.	(1,800)	4,976
Net	(1,797)	5,520
Per shr.	(0.03)	0.08

LTX Corporation

Q4 Ending July 31: ($000).

	2008	2007
Sales	$35,848	$30,114
Ops. Pft.	381	(4,473)
Net	630	(4,185)
Per Shr.	0.01	(0.07)

FYr. Ending July 31 ($000)

	2008	2007
Sales	$135,825	$147,639
Ops. Pft	(4,739)	(10,414)
Net	(600)	(10,666)
Per Shr.	(0.01)	(0.17)

MCT Inc.

FQ2 Ending June 30 : $000

	2008	2007
Sales	$2,963	$3,960
Ops. Pft.	(132)	(343)
Net	(685)	(280)
Per shr.	0.2)	(0.01)

Verigy, Ltd.

FQ3 Ending July 31 : $000

	2008	2007
Sales	$179,000	$204,000
Ops. Pft.	15,000	31,000
Net	18,000	30,000
Per shr.	0.18	0.30
Orders	$165,000	$298,000

ATE Company Qtrly Financial Reports

Verigy, Ltd.

Verigy said that its fiscal third quarter revenue was $179 million, up 10 percent sequentially, but down 12 percent YoY. Net for the quarter was $18 million or $0.29/share, compared with $14 million or $0.23/share in the prior quarter, and $30 million or $0.50/share in the prior year period.

On a product basis, SoC testers - including high-speed memory testers - accounted for $129 million of its revenue for the quarter; FLASH memory testers just $9 million and service represented $41 million.

Orders were $165 million, down 7 percent sequentially and down 21 percent YoY, Orders by region were: Asia-Pacific 81 percent, Americas 11 percent and Europe 8 percent. The orders split between IDM and fabless versus OSATs was 40 percent and 60 percent respectively, compared to 61 percent and 39 percent respectively last quarter.

Verigy's SoC tester revenues, including high-speed memory testers, was highest ever for this product line. It also said it had delivered more than 100 testers with nearly half coming from the Flextronics China facility. Sales of the 93K were fueled by a healthy demand for wireless, PC and consumer mix signal devices. It noted that it had three customers which accounted for 'greater than 10 percent of its revenue for the quarter. It indicated that Nvidia had represented about 20 percent, but would not name the other two.

Keith Barnes, Verigy chairman/CEO/president, noted: "We support high-speed memory applications from our SoC division. The high-speed memory market is characterized by devices with data rates in excess of 1 gigabit per second. The ATE revenue opportunity for this high-speed memory's is estimated to be about $60 million in 2008 and forecasted to reach about $200 million in 2010.

We believe we are well positioned to capture a significant share of this market. Our 93K HSM product is already being used in volume manufacturing to test devices running between 2 & 4 gigabits/sec and in engineering applications at virtually every high-speed memory manufacturer in the world. During the quarter, we introduced our HSM 93K 2200 system at the SEMICON West Trade show in San Francisco. This is the first tester available on the market capable of testing 64 devices in parallel at speed for final test and is upgradeable to a 128 site configuration by swapping channel cards." Barnes also noted that in Q3 it had received an order for a high-speed memory system which will be used for the characterization of GDDR5 devices and also won repeat orders from major DRAM manufacturers for testing DDR3 devices."

However, he said the company's FLASH memory tester sales of $9 million, while up $3 million sequentially, still declined precipitously YoY, "as memory manufacturers continue to take steps to preserve cash by cutting their CapEx budgets, delaying equipment purchases or postponing new fabs. These are actions have contributed to a historically low memory tester buy rate [percentage of revenues spent on test systems]. For calendar year Q2 it was less than 1 percent," Barnes claimed.

Barnes added: "We have won several new memory evaluations for engineering development and believe that these wins will eventually transition into high volume manufacturing orders at several key accounts.

Finally, Barnes said "In recent weeks, customers have become more cautious with their outlook and a few have pushed out of orders. As a result, we expect to see some softening in Q4 as reflected in our next quarter guidance. Revenue for the present (October) quarter is expected between $155 to $165 million and net is expected to be in the range of $7 to $10 million, or $0.12 to $0.17/share."

LTX Corporation

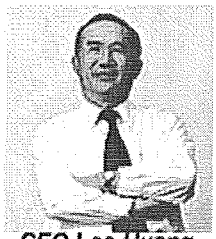
Reporting its last quarter and fiscal year before its merger with Credence Systems - said its sales for its FQ4, ended July 31, were $35.848 million, down 9 percent sequentially, but up 19 percent YoY. Its net for the quarter was $630,000, or $0.01/share. For the same quarter of F07 sales were $30.114 million and a loss of $4.185 million, or $0.07/share - 83 percent product and 17 percent service. Its orders for the quarter were $30 million. For the full fiscal 2008 year, its sales were $135.825 million compared to $147.639 million in the preceding fiscal year. Its loss for the year was $600,000, or $0.01/share, which included a tax benefit totaling $3.091 million or $0.05/share. For the prior fiscal year, its loss was $10.666 million, or $0.17/share, which included inventory and restructuring charges of $3.798 million or $0.06/share.

LTX said that after its merger was Credence Systems was completed on August 28, 2008, the combined company's revenues for the quarter ending October 31, 2008 is expected to be in the range of $60 million to $64 million. This is based on three months of LTX revenue of $30 million to $34 million and two months of Credence revenue of about $30 million. It did not provide any estimate of profit/loss for the combined companies, but said LTX, as a standalone company, is projected to have a loss of $0.06 to $0.02/share

On August 22 Credence announced revenues for its FQ3, ended August 2, were $62 million and bookings were $43 million. Credence also said that on August 25, it had received a letter from a purported representative of certain holders of its 3.5 percent Convertible Senior Subordinated Notes due 2010, [about $50 million plus accrued interest} taking the position that the merger would constitute a change of control and Credence would be required to offer to repurchase all outstanding Notes. Credence and LTX said they are reviewing the letter and their response thereto.

FOCUS ON Chroma

Chroma ATE, headquartered in Taiwan's Hwa-Ya Technical Park, was founded Nov, 1984 by its chairman/CEO Leo Huang. The company offers a wide range of test and measurement products including VLSI and SoC test systems, Automatic Power Supply Test Systems, Programmable AC Power Sources, DC Electronic Loads, PXI Test Instruments, Video Testers, Hipot Testers, and LCR Meters.


CEO Leo Huang

In 2007 the company reported sales of US$131.5 million and employs about 1,123 worldwide. It became a publicly-held company in 1996 on the Taiwan Stock Exchange (2360).

It is the dominant player in Taiwan for power supply, video and color, and passive component test equipment and the primary test equipment supplier to major LCD, LCM (modules), and LED makers in Taiwan.

Chroma established a U.S. subsidiary in Irvine, CA in 1994 that is focused on Automatic Power Supply Test Systems, Programmable AC Power Sources, Video Testers, Electronic AC and DC Loads, and PXI Test Instruments and Chassis products. Earlier this year it set up a subsidiary in Japan.

While power supply testers remain its "foundation" representing about one-third of its revenue, semiconductor test systems is its fastest growing product line - rising from 5 percent of its total revenue to more than 25 percent in the last three years.

It's expected that in 2008 its IC tester business will reach about $45.5 million or about 28 percent of its total revenue and exceed power supply tester revenue next year.

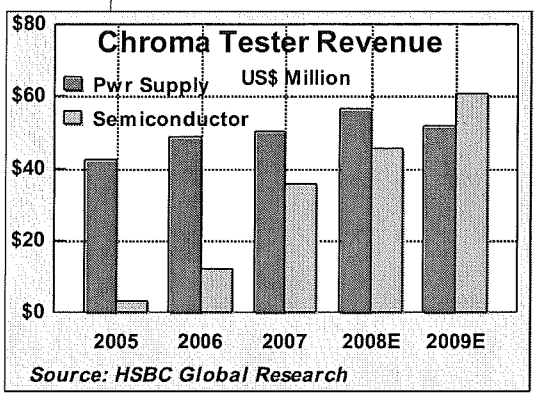
Chroma Ate: Sales by Segments

	1H07	1H08	YoY
Pwr Sup.	$23.08	$30.50	32.2%
Video	$6.94	$5.13	-26.0%
General	$6.71	$7.78	15.9%
LCM test	$8.94	$4.94	-44.8%
IC test	$13.82	$20.40	47.7%
LED test	$1.23	$2.10	71.1%
Total	**$60.72**	**$70.85**	**16.7%**

Source: Company July 2008

Chroma's IC testers are described as 'low-cost', featuring data rates in the 50/100 MHz range, and are targeted at final package test. However, it expects to expand its business into the wafer-sort segment this year. Its latest product, the Model 3650 SoC test system (side bar) is typical of its present products

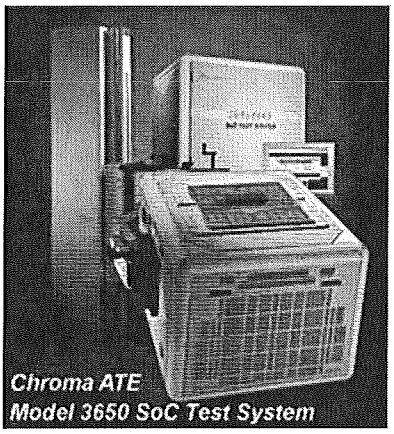
Chroma is cautiously optimistic about the second half of 2008, saying that it expected delays in some orders and that quarterly sales should peak in the fourth quarter. Due to the fact some customers are reluctant to move to China, it plans to strengthen its operations in the US and Japan.



Source: HSBC Global Research

Chroma has impressive [for tester makers] 55+ percent gross and 30+ percent operating margins. That makes it "one of the best investments in the semiconductor and test industries," in the opinion of HSBC Global Research analyst Steven Pelayo.

He adds "As semiconductors become less expensive versus the expensive equipment used to test them, more chipmakers are embracing a combination of lower capital cost and more primitive 'functional test' methodologies using equipment like those offered by Chroma."


Chroma ATE
Model 3650 SoC Test System

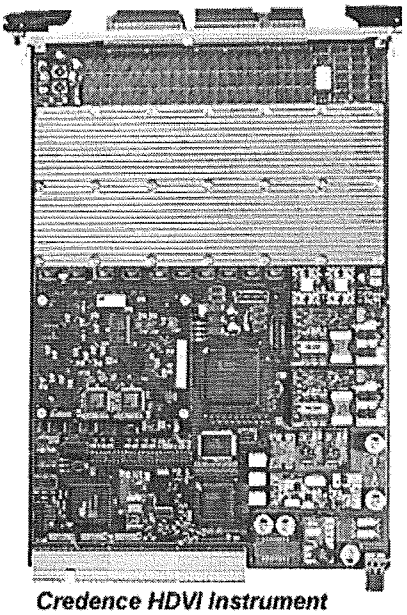
Key Features

- Air-cooled, small footprint tester-in-a-test-head design
- 50 /100 MHz
- 512 digital I/O pins
- 16/32 MW vector memory
- 16/32 MW pattern instruction memory
- Multi-site testing up to 32 sites
- Per-pin test architecture
- Up to 8 16-bit ADDA channels
- Up to 2Gbit X 8 CH scan depth
- ALPG option for memory test
- Up to 32 high-voltage pins
- 32 high-performance DPS channels
- Overall timing accuracy < ±550ps
- Test template for test program creation
- Test program and pattern converters for other platforms

Credence Systems unveiled the latest addition to its family of instruments for its Diamond test platform. The 72-channel HDVI (High Density Voltage/Current) instrument is targeted at significantly reducing the cost of test by enabling larger numbers of sites to be tested in parallel.

The company said the HDVI is production ready and customer shipments have started. Among the applications already in progress:

- 8 site production test program for large GPS baseband process (reduced capital cost ~30%)
- 16 site Bluetooth benchmark (reduced capital cost ~40%)
- >100 site (strip test) (reduced CoT ~30% vs. competition)



Credence HDVI Instrument

The HDVI provides up to 432 channels on the Diamond 10, and 1728 channels on the Diamond 40. When combined with the Diamond platform's other high-density instruments - it reduces the number of test cells needed on the production floor.

The HDVI contains 72 channels that can be operated in one of two modes: (1) Voltage/Current Supply (VIS) and (2) Precision Analog Source (PAS). The VIS mode offers 72 channels of general purpose, four-quadrant V/I capability for up to +/-7V and a maximum of +/-2A. In the PAS mode, each channel is capable of sourcing user-defined analog waveforms with very high accuracy for driving analog inputs of microcontrollers and embedded ADCs to perform INL and DNL tests.

Key HDVI Features

- Built-in, high-bandwidth input matrix allows external instruments to connect to multi-use DUT pins and eliminate loadboard components.
- Trigger control for source and measure memory synchronizes operation with tester or DUT events.
- High-current performance on large number of pins provides coverage for the growing embedded power management features in battery-driven consumer products.
- High-accuracy voltage (<+/-0.9 mV) and current (<+/-80 nA) measurements enable reliable testing of sensitive reference pins.
- Per channel cost $1500

Key Specifications

Voltage/Current Supply (VIS mode)

- 72 channels; 4 quadrant
- ± 7V @ ± 256mA
- Low ±15μA range to ± 2A
- 4K source, 1K measure memory per channel, event triggered

Precision Analog Source (PAS mode)

- 2 independent precision analog sources
- Individual channel gain & offset cal
- 3V, 6V ranges with 16 bit resolution
- 128K waveform memory/source
- 1Hz to 100kHz sample rate, event triggered

FormFactor Unveils *Its RapidSoak*

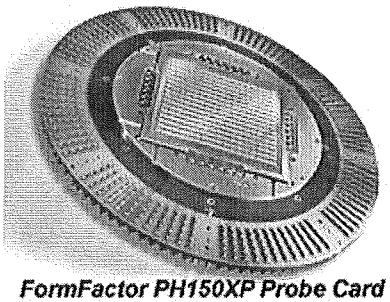
FormFactor said it has developed a new technology to enhance its advanced wafer probe cards that offers improved performance and productivity. The new technology, known as *RapidSoak,* is designed to reduce the time required for the probe card to reach thermal stability, between wafer lots, after card maintenance/cleaning and after the installation of a new card.

The technology involves the inclusion of heating and temperature sensor elements on the probe card. These are integrated onto the probe card as part of the card design and manufacturing process.

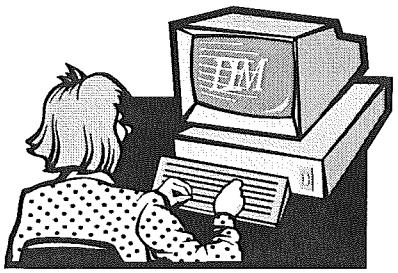
"Test temperature recalibration is necessary during probe card installation, wafer exchanges, lot changes and probe card maintenance. Depending on the device type, test times and manufacturing volume, these 'soak' times can amount to hours of lost productivity each day," the company noted.

"As we reduce wafer test time with full-wafer contactors, soak time has a larger impact on test cell utilization," stated Stefan Zschiegner, VP of the DRAM product business unit at FormFactor. "With our RapidSoak technology, we can reduce soak time — in some test cell configurations very dramatically — adding productivity back to the test cell and increasing our customers' throughput."

The RapidSoak feature is available now as an option on new FormFactor Harmony and PH150XP probe cards.



FormFactor PH150XP Probe Card



Is Design Now the Major Chip Driver?

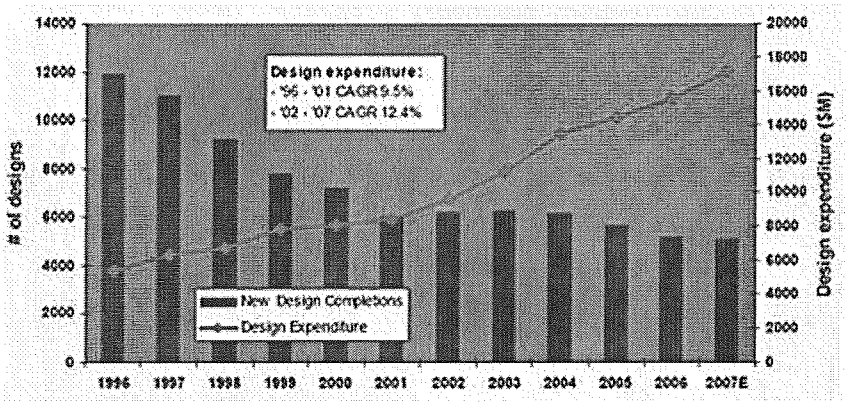
Through most of the history of the semiconductor its growth was driven by advances in lithography. However, arguably now chip design is driving the supply chain - higher fab efficiency (reduced cost per square inch of capacity) has allowed more complex designs to be developed.

Through '00 the average design cost per transistor was following Moore's Law. Design cost reductions averaged 19 percent per year between '92 and '00. This slowed to 5 percent between '01 and '06 as the industry failed to adjust to the process transition from microchip to nanochip {the move to subwavelength lithography or, the printing of feature sizes that are smaller than the wavelength of light} and not recognize that Designing for Manufacturability (DFM) would require more investment.

As VLSI Research president, Dan Hutcheson, put it at SEMI's *Silicon Valley Lunch Forum* in Santa Clara CA last month: "In the 1980s, design separated from process and one no longer needed to know process, just electrical engineering. Today, designers don't know electrical engineering; they're software programmers, and the design tool does everything.

Hutcheson also note that one result of the 2001 crash was that chip companies stopped heavy investment in design tools, cutting design tool companies' profits. "This reduced efficiency, in terms of a transistor's design cost. Design costs will escalate rapidly, making it difficult for chip manufacturers to be profitable because they cannot differentiate their products."

Hutcheson noted that design expenditures are growing, but the number of designs is declining.



This means a drop in differentiation and value," he warned. "At present, the value of silicon for the U.S. semiconductor industry is three times what it is in rest of the world because we have a high degree of differentiation. If we cannot design we're in trouble because, as designs decline, so do revenues and ASPs." Even so, its worth noting that from '96 to '01 EDA expenditures by chipmakers grew at a 9 percent CAGR. From '02 to '07 they grew at a rate of 12.4 percent.

The problem is that when you are printing sub-wavelength features "what you see is not necessarily what you get.". This means it becomes very important that chip designers understand the deficiencies in process and the process people understand the adjustments necessary to make a design manufacturable. This is a huge issue, particularly when you consider that the number of designers only grows at 1 percent per year.

Arguably these rapidly rising EDA expenditures are stacking the deck against fabless houses that are making small run designs. For the fabless houses it is very, very expensive to design at 90nm and below. Add to the design cost the fact that foundries are backing away from aggressive scaling (due to cost and poor yields)."

And. Hutcheson believes you have a situation where the foundry business model may have peaked.

He said: "Even if the foundries have capacity, the high cost of design creates a scenario for slower revenue growth across a broad swath of the industry If this plays out as expected we anticipate that fabless and fab-lite chipmakers will end up paying higher prices for foundry capacity. To a certain extent this may come as a surprise to the chipmakers such as TI and AMD that are transitioning to the fab lite model." He argues that "limited scaling means limited financial returns. Nimble logic IDMs will be able to take advantage of weaker fabless suppliers. Those that want to produce smaller, highly scaled, device runs are going to find it more difficult to get capacity."

FINANCIAL REPORTS

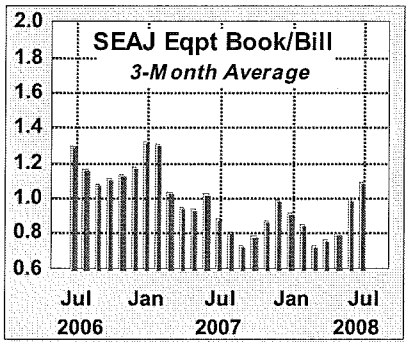
LogicVision, Inc..

Q2 Ending June 30: ($000).

	2008	2007
Sales	$3,027	$3,083
Ops.	(1,057)	(1,245)
Net	(997)	(1,120)
Per Shr.	(0.10)	(0.12)

EDA STOCKS

COMPANY	Ticker	Close 08/29	Change Month	52 Week High	52 Week Low
Cadence	CDNS	$7.99	8.1%	$22.64	$6.90
LogicVision	LGVN	$1.19	-8.5%	$3.00	$0.99
Mentor	MENT	$12.20	-12.1%	$16.50	$7.51
Synopsys	SNPS	$21.53	-10.4%	$29.11	$19.59
Avg. Change			-5.7%		



Japan Chip Eqpt. B/B Hits 1.09 in July '08

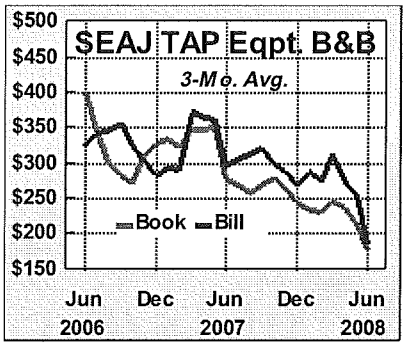
The SEAJ said that Japan's chip equipment makers reported three-month average bookings for July 2008 of ¥92,308 million (US$871.55 million), up 5.4 percent sequentially but down 37.2 percent from ¥147,058 million posted in July 2007.

The three-month average of billings in July 2008 was ¥84,718 million (US$799.88 million), down 4.0 percent from the June 2008 level of ¥88,283 million but down 49.1 percent down the July 2007 billings of ¥166,458 million.

The resulting July book-to-bill was 1.09 - the first time in thirteen months that figure was above unity.

JAPANESE ATE STOCKS

INDEX	Ticker	Close 01/31	Change Month
NIKKEI 225	N225	13,592	-11.2%
Advantest	6857	2,335	-26.6%
JEM	6855	1,016	-7.2%
MJC	6871	3,900	3.2%
TEL	8035	6,360	-7.3%
TSK	7729	2,135	-21.9%
Yokogawa	6841	1,029	-16.2%
Average Change in January			-12.7%



Japan June TAP Eqpt. B/B at 0.72

(Note: The SEAJ reports its actual monthly chip equipment book & bill data about 3 weeks after it reports its 3-month avg. total equipment B/B.)

Japan's Test, Assembly and Packaging (TAP) equipment makers reported actual bookings for June 2008 of ¥17,433 million (US$163,265 million), down 9.4 percent MoM and down 46.9 percent YoY. Actual billings in June were ¥24,152 million (US$226.2 million), up 32.7 percent MoM, and down 44.7 percent YoY. Japan's actual TAP book-to-bill for June was 0.72.

On a three-month average basis, Japan-based TAP equipment makers' June 2008 bookings were ¥18.347 million (US$175.61 million), down 6.9 percent MoM, and down 34.6 percent YoY. Three-month average billings were ¥19,336 million (US$185.1 million), down 14.2 percent MoM and down 8.6 percent YoY. The resulting 3-month average book-to-bill ratio for Japan TAP makers was 0.95 for June 2008.

For the first six months Japan's actual TAP equipment bookings were down 40.8 percent YoY, while billings were down 34.8 percent YoY.

In comparison, Semi reported that (revised) No. America-based Test, assembly and packaging (TAP) equipment bookings (three-month average) in June 2008 were $228.9 million in June, up 6.5 percent MoM, but down 6.5 percent YoY. Billings were $211.6 million, up 1.9 percent MoM, but down 14.1 percent YoY. Semi's TAP B/B was 1.08 for June 2008.

Top Taiwan Foundry Considering Layoffs

The cutbacks that have been seen at U.S. chip and chip equipment makers may be spreading to Asia, according to recent reports from Taiwan.

United Microelectronics Corporation (UMC), the world's number two chip foundry, has recently had a large-scale upper management personnel reshuffle. A second stage reshuffle at middle management is expected to take place soon and reportedly UMC is considering laying off about 10 percent of its employees across the board

In contrast to past years, where leading foundries such as Taiwan Semiconductor Manufacturing Company (TSMC) and UMC usually recruit additional employees to meet seasonal demand upsurge, they have reportedly kept a relatively low profile in the hiring market this year,

In addition, the weak demand in the semiconductor industry is also spreading to the chip equipment side of the market. Since equipment bookings are low, as they are in the U.S. and Japan, employees at some equipment vendors have at least begun to eliminate overtime work.

Among all major foundries, only TSMC has guided that its utilization rate will post any sequential growth in the third quarter, whereas UMC and Vanguard International Semiconductor (VIS) both trimmed their utilization rate guidance to about the 80 percent level.

The top four foundries, namely TSMC, UMC, Chartered Semiconductor Manufacturing and Semiconductor Manufacturing International Corporation (SMIC), have also all announced they will maintain their capital expenditure CAPEX static or actually trim it YoY in 2008.

As an example, the largest foundry, Taiwan Semiconductor Manufacturing (TSMC) announced that its capital expenditure budget for 2008 is expected to be around $1.8 billion, compared with $2.6 billion it spent in 2007.

The 39th International Test Conference (ITC) will be held in Santa Clara, CA on October 28-30, 2008 at the Santa Clara Convention Center.

This year, the International Test Conference technical program, together with other Test Week 2008 events, will focus on "breakthrough ideas to address the challenges of providing high-quality, cost-effective tests for IC boards and systems." The program will focus on the latest advances in such hot topics as design for manufacturability, power-aware test, recent advances in delay test, logic diagnosis, silicon debug, and high-quality test methods. In addition, traditional topics such as analog, mixed-signal, RF, microprocessor test and DFT-as well as defects, memory, ATE and board test will be also presented.


General Chair Doug Young

The conference begins with the plenary session and a keynote address by Mike Lydon, Cisco's VP for Technology and Quality, Global Supply Chain Management, titled *Managing Test in the End-to-End, Mega Supply Chain.* He will discuss how today's "connected" environment has created significant growth opportunities in the electronics industry.

The technical program contains 35 paper sessions, and is supplemented with a lecture series and advanced industrial practices sessions on high-speed interface testing, board testing, automotive test and a special joint session with the *Autotestcon* conference on system test.

This year's panels begin on Monday afternoon with a special panel titled *Power-aware DFT-Do We Really Need It?.*

Five additional panels will cover analog test technology, data compression as a future-proof solution, debugging war stories, benefits and economics of yield learning, and a showdown between universities on up-to-date test research.

ITC 2008 Exhibitors

Aehr Test	M & M Specialties
Antares ATT	MEI
Ardent	Mentor Graphics
ARM	Asset InterTech
Atrenta	Nano ISolutions
Azimuth	NHK Spring
BucklingBeam	Optimal Test
Cadence	Phoenix Test
Carsem	Pickering
Cascade	Pintail Tech
Centellax	Presto Eng
CMR Summit	Probe Logic
Corad Tech	Proligent
Corelis	Protos
Credence	Q-Star Test
Dynamic Test	QualiSystems
EE Evaluation.	R&D Circuits
Electroglas	Reid-Ashman
ELES Eqpt	Roos Instruments
ERS America	Rucker and Kolls
Evans Analy.	Sanyu Electric
Everett Charles	STC
Exatron	Siliconaid
Finley Design	Simutest
Focused Test	Springer Media,
FormFactor	SV Probe,
GE Fanuc	Synopsys
Geotest-Marvin	SynTest Tech
GOEPEL	Taconic
Hamamatsu	Teledyne Relays
HiLevel	TeraVicta
Inovys	Teseda
Integra Tech	T&M World
Integrated Test	Test Coach
Intellitech	Test Insight
inTest SV	TEL America
JD Instruments,	TSSI
Johnstech	Unitechno USA
JTAG Tech	Virage Logic
Lambda	WorldTest Sys
LogicVision	Yamaichi

New for 2008 are 'embedded tutorials' that will be conducted during the technical program and offered free of charge to all registered ITC attendees. Robert Daasch of ICDT Laboratory will present an introduction to statistics and their uses in semiconductor test, specifically, outlier screening. The other, presented by Gordon Roberts of McGill University, will describe the basics of mixed-signal production test.

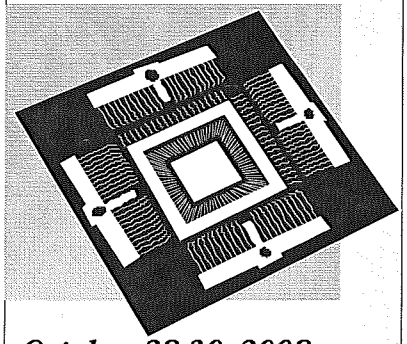
Also, poster sessions will return to ITC providing an opportunity for late-breaking results to be presented and receive feedback. The poster session will be held during the post-panel party on Wednesday, October 29.

Closing out Test Week are three workshops to choose from on design for reliability and variability, defect- and data-driven testing, and ATE Vision 2020. These workshops provide in-depth and up-to-the-minute views of work in these important test areas.

An exhibit floor will feature the newest equipment, software and services from all over the world for solving testing problems.

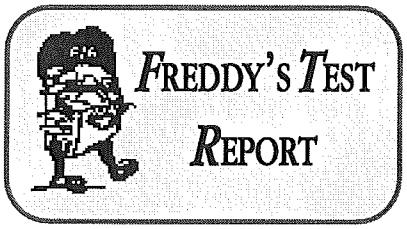
ITC's Advance Program and on-line registration are available on its Web site at **www.itctestweek.org.**

ATE/DFT MEETINGS



October 28-30, 2008
International Test Conf.
Santa Clara Convention Ctr.
Santa Clara, CA
www.itctestweek.org

December 3-5 2008
SEMICON Japan
Makuhari Messe
Chiba, Japan
www.semiconjapan.org



INDUSTRY

IDC estimates that the PC microprocessor market grew 3.1% in unit shipments in the June quarter, but price competition drove revenues down 4.5%. "**Intel**'s processor shipments grew nearly 4.3% sequentially and 20.8% YoY, while **AMD**'s processor shipments were about flat," it said.

iSuppli said DRAM bit shipments grew 17% sequentially during Q2, blowing its prediction of 10%," "The good part of the story is that the PC market has been sound. However, oversupply may be inevitable in Q3 due to OEMs' aggressive inventory buildup during Q2," it added.

IC Insights said that overall average chip prices will fall by about 1% in 2008 - a marked improvement over 2007 when ASPs dropped by about 5%. The difference is due to the fact that chip suppliers are scaling back on capital expenditures and foundries are running at nearly 100% utilization. It expects that chip prices will be flat in 2009, but then increase 1% in 2010, 2% in 2011 and 3% in 2012.

COMPANIES

Verigy said that, **Suzhou CAS** (Chinese Academy of Science) Integrated Circuit Design Center (SZICC), a Chinese government sponsored full-service IC design, test and training facility, has purchased a Verigy V93000 SoC tester to support the test requirements of the growing number of local fabless companies.

Cadence Design Systems has withdrawn its $1.5 billion cash offer to buy Mentor Graphics. It said "Mentor's executives and board wouldn't discuss the substance of the deal with them," Mentor however said, "Cadence was having trouble raising funds for the deal."

NanoNexus, the San Jose, CA-based maker of MEMS probe cards, has closed its doors and is in the process of liquidating its assets. The company, founded in 1999 had raised a $70 million in venture capital,

Credence Systems has signed an agreement with **MVTS Technologies** (Carlsbad, CA) for the support of seven Credence legacy products, *Vista, Duo, Quartet, Octet, SC, Kalos,* and *EXA*.

LogicVision has named **Avant Technology** as its distributor in Taiwan and **Amblot SARL** as its representative in southern Europe.

PEOPLE

Mark Moore has joined **Teseda** as its VP of Engineering, based at the company's new Silicon Valley facility. Previously, he had been responsible for the development of the **Credence** *Sapphire* Test System.

Jong Ho Yoon has been named to head **SV Probe**'s new subsidiary, **SV Probe Korea**. He had been with **Mico TN**, a Korean probe card maker.

Kena Pegram has joined **R&D Circuits** as its West Coast Regional Sales Manager.

Mike Kondrat has been named VP, Marketing and **Anand Nambiar,** VP, Operations for **Cascade Microtech.**

Elke Eckstein, after less than two years as VP for manufacturing at **AMD**'s Dresden site, has left to become COO for **Osram Opto Semiconductor** in Regensburg, Germany.

Bob Merritt and **Sherry Garber** have left **Semico Research** to start a new memory research firm called **Convergent Semiconductors.**

Professor Eicke Weber has been named to **SEMI**'s Intl. Board of Directors. He director of the **Fraunhofer Institute for Solar Energy Systems** and a professor at the **Albert-Ludwig University** of Freiburg, Germany.

EXHIBIT 6

A 400 Personnel Sampling of the ATE Industry

Date	Employee Name	Previous ATE Company	Position	New ATE Company	Position
8/1/2007	Aart J. de Geus	Synopsys	Chairman/CEO	Applied Material	Board of Directors
7/1/1997	Al Hutton	Advantest	Sales Operations	Prime Yield Sys	
10/1/2002	Allan Calamoneri	ASAT		Test Spectrum	
9/1/2000	Allen Sheng	LTX	Sales/Branch Mgr.	GuideTech	VP of Asia Operations
9/1/2007	Amir Aghdaei	Agilent	GM/VP of Measure	Credence Systems	Sr. VP of Field Ops
10/1/2003	Andre Berar	Credence Systems	VP	Kulicke and Soffa	VP for Test Packaging
8/1/1998	Anne Wagner	Sun and National Semi	Mktg. executive	Mentor Graphics	VP of Mktg.
6/1/2007	Antonio Guzman	Teradyne	Sales Engineer	TEAM A.T.E.	Represent Mexico
9/1/2005	Armagan A. Akar	LogicVision	Managing Director	Tesada	CEO
4/1/2002	Art Downey	Ando/Credence		Schlumberger SS	Mgr. of calibration grp.
12/1/1997	Ashwin Ballal	Keithly Instruments	Marketing Manager	Elecgtroglas	Product Marketing Mgr.
9/1/2001	Barry Baril	IMS	Founder/CTO/VP Eng.	Credence Systems	CTO
1/1/1997	Bart Freedman	Schlumberger		Credence Systems	VP of Strategic Sales
11/1/2006	Bernard Sutton	Teradyne		CloverTest Associates	Consultant
12/1/2007	Bernie Blegen	Credence	VP of Finance	Shutterfly	VP of Finance
5/1/1999	Bill DeWilkins	Teradyne		Integra Technologies	Mgr. of Linear Test Eng.
3/1/2005	Bill Frerichs	D.A. Davidson & Co.		Synopsys	VP of Market Research
2/1/2000	Bill Woods	GE Electronics	ATE product mgr.	Comdisco	Strategic Alliances mgr.
2/1/2003	Bob Chamberlain	Starview Technology	co-founder	ESI	VP customer operations
5/1/2000	Bob Durstenfeld	Agilent Tech	Manager of Test	KVO Public Relations	
1/1/1997	Bob Grant	LTX	VP of Software	Schlumberger	Software Management
6/1/2001	Bob Helms	Texas Instruments	Dir. of Silicon Tech	International Semtech	President and CEO
6/1/2001	Bob Huston	Credence	VP of Test Technology	3MTS	
9/1/2008	Bob Merritt	Semico Research		Convergent Semi	
6/1/2007	Bob Moore	Dubai Silicon Oasis	Dir. Of Sales	Silicon Boder Dev.	VP of Bus. Dev.
12/1/1997	Bob Oakley	Advantest America	President	TMT	Board of Directors
1/1/2007	Bob Sandberg	Delta Design	Sales Manager	inTEST	Sales Manager
9/1/2002	Bob Watson	ASAT		United Test and Assem.	Director of Sales
11/1/2003	Brian Bachman	Axcelis Technologies	CEO	K&S	
1/1/2006	Brian Beattie	SupportSoft	CFO	Synopsys	CFO
10/1/2004	Bruce Griffing	Dupont Photomasks		Kulicke and soffa	VP of Engineering
7/1/1999	Bruce McWilliam	nChip	Founder	Tessera	Pres./CEO
9/1/1999	Bruce P. Delmore	Strategeos Group	Pres. of Consulting	Photon Dynamics	VP of Marketing
9/1/2003	Bruce R. Wright	Ultratech	CFO	Credence Systems'	Director
1/1/2000	Bruce Stromstad	Cirrus Logic	VP of Manufacturing	ChipPAC	VP of Manufacturing
4/1/2002	Casey Swan	Wavecrest	Dir. Of Asia Sales	Schlumberger Saber Grou	Sales mgr. for Fabless
10/1/1997	Charles E. Cump	Viewlogic	Co-founder, Pres.	Summit Design	VP of N. American Sales
9/1/2007	Chetan Desai	Credence Systems	GM/VP of ATE	Formfactor	Lead Sapphire
10/1/2003	Chris Baxter	Credence Systems		LTX	Global Account Manager
10/1/2004	Chris Buckley	ChipPAC	VP of SE Asia	MCT	Sr. VP of Worldwide Sales
10/1/2000	Chris Helland	Schlumberger	VP of Memory Test	KLA-Tencor	Director of Engineering
5/1/1997	Chris Menicou	LTX's Trillium	Director of Quality	Credence Systems	Director of Quality
4/1/1997	Chris Noe	Teradyne		Comdisco Eletronics Grou	ATE Product manager
12/1/1999	Chris Noe	Comdisco		Kinetix Test Systems	VP Sales
6/1/2001	Chris Noe	Kinetix Test System	VP of Sales	Aehr Test Systems	VP of Sales
8/1/1998	Chuck Miller	Credence Systems	Engineering Manager	Formfactor	Engineering
3/1/2001	Clive McGovern	Litton Precison Products	GM	ESI	European Sales Manager
1/1/1997	Clyde Armstrong	LTX		Credence Systems	VP of Sales
11/1/1999	Clyde Armstrong	Credence Systems	VP of Sales	Inovys	CEO

12/1/2004	Colin Ritchie	NPTest	Mgr. Invest Relations	Inovys	VP of Marketing
10/1/1998	Curtis Wozniak	Electroglas	Chairman/CEO	SEMI/SEMATECH	Board of Directors
5/1/1999	Dale Buxton	LTX		TMT	Asian Sales Manager
6/1/1998	Dale Olstinke	Frequency Electronics	Executive VP	LogicVision	VP of Sales
11/1/1998	Dana Brown	LTX	Motorola Acc. Mgr	Advantest	
1/1/2001	Daniel (DJ) Hill	Cerprobe	VP and COO	D.J. Hill & Associates	Founder
3/1/2008	Danny Chiu	Spirox	Sales Management	Intntl. Test Solutions	Applications Manager
3/1/2004	Dave Bayly	Teradyne	Regional Sales	Inovys	VP/Sales/Marketing
5/1/1998	Dave Bullis	Synopsys	Sr. VP	Data I/O	CEO and President
7/1/1998	Dave Dowding	Microchip		TSSI	Dir. Test Technology
4/1/1997	Dave Flaningan	Credence Systems	Head of Asian Ops	Genus	
3/1/2001	Dave Ring	Entegris	President	LTX	Executive VP
4/1/2002	Dave Sulman	Teradyne	VP		
8/1/1998	David Brinker	IMS	GM	Webrige	CFO
7/1/2005	David Churchill	Tektronix	Executive	Agilent Tech	VP/GM
1/1/2001	David DeVillez	Steag RTP	GM of Operations	GuideTech	VP of Operations
6/1/1998	David Flamingam	Genus	VP of Operations	IMS	Dir. Of Sales
5/1/2005	David Flaningam	Credence Systems	Vice President	Cort Software	President
1/1/2006	David House	Brocade Comm.	Chairman	Credence Systems	Executive Chairman
2/1/1997	David L. Brinker	TVIEW	President/ CEO	IMS	GM.
7/1/1997	David M. Sugishita	Actel	VP of Finance	Synopsys	Sr. VP of Finance
11/1/2001	David Ring	LTX	Executive VP of Sales	Phymetrix	CEO
12/1/2001	David Ring	Entigris	President	LTX	Executive VP
5/1/2005	David Van Loan	ECT	President	Dover Technologies	President
1/1/1999	David W. Smith	Quad Systems		ESI	VP/GM
9/1/2000	Davoid L. Angel	The Fabless Semi Assoc	Chairman	Castlemont	Presidnet/CEO
10/1/2006	Dean Van Druff	Credence Systems		KVD	VP of Sales
5/1/2002	Dean VanDruff			SZ Testsystems	VP of Sales
5/1/2004	Dean VanDruff	SZ Testsystems	VP of US Sales	Credence Systems	Product Marketing
4/1/1998	Dennis A. Legal	Aseco	VP of engineering	Cerprobe	VP of R&D
5/1/2004	Dennis Malloy	Kulicke & Soffa	VP of Sales	Advantest America	N. American Sales Mgr.
7/1/2008	Dennis Nelson	Teradyne		Verigy	
4/1/1998	Dennis Wolf	Centigram Communication	Senior VP and CFO	Credence Systems	Senior VP and CFO
4/1/2005	Dennis Wolf	Credence Systems	co-president/CFO	Hercules Technology	CFO/VP operations
4/1/2006	Dipanjan Deb	Credence Systems	Board of Directors		
6/1/1997	Don May III	Delta (COHU)	VP of Sales	K&S	VP of Sales
5/1/2006	Don R. May III	K&S	VP of Sales	Eagle Test	Sr. VP of Sales
1/1/2002	Doug Day	SpeedSim	VP of Sales	Teseda	VP of Sales
2/1/2001	Doug Young	Cerprobe	VP of Sales	SV Probe	VP of Sales/ Mktg.
9/1/2003	Dov Oshri	Orbotech	VP of Finance	STATS	CFO
12/1/1999	Dr. Arnon Gat	AG Associates	Founder	GuideTech	Presidnet/CEO
1/1/2000	Dr. B.J. Han	Anam Semi	Dir. of Prod. Dev.	STATS	CTO
8/1/1998	Dr. Edmund K. Cheng	Anagram	President/CEO	Synopsys	VP of Research and Dev.
7/1/2005	Dr. Graham Siddal	Credence Systems	Exec. Chairman	ReVeta	Board of Directors
7/1/1997	Dr. James Fiebiger	VLSI Technology	President	Zycad	President
10/1/2006	Dr. Ki soo Hwang	Core Logic	President/CEO	FSA	Council
2/1/2008	Dr. Mario Ruscev	Schlumberger		Formfactor	Board of Directors
10/1/2004	Dr. Michel Villemain	NPtest	VP/GM Probe Systems	KLA-Tencor	VP of Metrology
12/1/2006	Dr. Ping Yang	TSMC	VP	Credence Systems	Board of Directors
11/1/1998	Dr. Richard S. Sidell	ESI	Dir. Product Eng.	Aseco	VP, Chief Technologist
9/1/1997	Ed Chang	Trilium (LTX)	Founder	ECTS	Founder
6/1/2006	Ed Rogas	Teradyne	Sr. VP	Photon Dynamics	Board of Directors
2/1/2000	Ed White	HP		SEMI	Program mgr.
1/1/2003	Ed Zander	Sun Microsystems	President	Seagate Technology	Board of Directors
5/1/2004	Eddie Kazama	Mitsubishi		JEM America	President/COO
2/1/2008	Edward C. Grady	Brooks Automation	President/CEO	Electro Scientific	Board of Directors
11/1/2006	Edwin J. Gillis	Synamtec	Sr. VP	Teradyne	Board of Directors

6/1/2002	Elwood Spedden	KLA-Tencor	VP	Photon Dynamics	Board of Directors
2/1/2003	Elwood Spedden	Credence Systems	President	Photon Dynamics	President/CEO
1/1/2001	Eric Scheidtmann	Amkor Technology	VP of Sales	Tessera	VP of Technology
6/1/2008	Eric Wilms	Schlumberger		Cascade Microtech	Director
1/1/2002	Eugene White	Amdahl	Retired CEO	Nextest Systems	Board of Directors
1/1/1999	Frank Sumner	Schlumberger	Sales Position	Aseco	Sales Manager
2/1/2004	Frank Sumner	Exatron		MCT	VP for US Sales
4/1/1997	Gary Bowers	Schlumberger ATE		Credence Systems	Regional Sales Manager
5/1/1998	Gary Breton	Amkor Technology		ChipPac	VP and Managing Director
5/1/2004	Gary Gillette	Credence Systems		GuideTech	VP of Engineering
6/1/1997	Gary L. Herd	MCT	Nat. Sales Manager	Aetrium	Regional Sales Manager
4/1/2000	Gary Rummelhoff	Adventest America	CFO/secretary	Atpos.com	CFO/VP operations
10/1/2002	Gay McFarren	K&S		Probe 2000	VP of Sales
3/1/2002	Geir Eide	Mentor Graphics		Teseda	Technical Marketing Eng.
1/1/2008	Geoff Wild	Nikon Precision	CEO	Cascade Microtech	CEO
9/1/1999	George Chamillard	Teradyne	CEO	Fabless Semi Assoc	Board of Advisors
7/1/1998	George Hoedeman	Micro Vision	President/CEO	Wavecrest	VP of Sales
9/1/2002	Gilluame d'Eyssautier	IBM Technology Group	VP	Cadence Design	VP/GM of Operations
9/1/2004	Glen S. Fukushitma	Cadence Design Systems	Chairman/Pres./CEO	NCR Japan	Co-President and Director
1/1/2001	Glyn Daview	KLA-Tencor		Credence Systems	VP of Marketing
8/1/2001	Gordon D. Robinson	Credence Systems	Sr. Tech. Staff	3MTS	Senior Member
9/1/2000	Graham Siddall	Credence Systems	President/CEO	NewMillennia Solution	Board of Director
10/1/1999	Greg Johnson	ASAT		Signetics High Tech.	
7/1/2004	Gregory Perkins	Advantest	Management	Aehr Test Systems	VP of Sales
4/1/2008	Haim Shani	NICE Systems	CEO	Optimal Test	Board of Directors
4/1/2008	Hal Lasky	IBM/Sequent Computer		STATS Chip-PAC	Ex. VP
12/1/1997	Harold Vitale	LTX	Sr. VP	Credence	Chief Engineer
6/1/2002	Harry Rozakis	ChipPAC	CEO	ASAT	CEO
2/1/1997	Henry Verheyen	Aptix	VP of engineering	Viewelogic	VP
2/1/2001	Henry Wong	Cerprobe	VP/GM	SV Probe	Partner
3/1/2004	Herb Hulseman	Analog Devices	Staff Engineer	Eagle Test Systems	Sr. Applications Engineer
7/1/2001	Hideo Sakane	Mitsubishi		JEM	President/CEO
1/1/1997	Holly Stump	EDA Companies		IKOS Systems	Dir. Of Product Marketing
9/1/1998	Howard Snyder	GE Capital Electronics	Regional Manager	Team A.T.E.	President
3/1/1998	Ian Pearce	VidaMed		Western Equiq. Dev.	Controller
4/1/1998	Irv Wilson	ESH	Marketing Manager	LTX's	Sales Operation
2/1/1997	Jack Barnes	LTX/Trillium	Sales mgr.	GE Capital Electronics	
12/1/1998	Jack Kessler	Amkor Technology	Dir. Of Test Tech.	Concepts Unlmited	Founder
6/1/2005	Jack Sexton	Credence Systems	Corporate Controller	Ultra Clean Holdings	VP/CFO
1/1/2000	Jackie Tubis	Schlumberger	President	SEMI	Board of Directors
11/1/1998	James Glaze	SIA	VP of Technology	LL National Lab	
11/1/2002	James Hogan	Cadence Design Systems		Artisan Components	
1/1/2002	Jan Heald Robinson	Credence Systems		Tesda	VP of Finance
9/1/1999	Jan van Limburg	Salland Eng. B.V.	CEO/Founder	Van Limburg Eng..	Founder
4/1/2008	Jean Bernard Vernet	Rio Tinto	Dir. Of Risk	Formfactor	CFO
10/1/2000	Jean-Luc Pelissier	High Connection Density	President	Schlumberger	VP of Mktg/Bus Dev
10/1/2007	Jean-Luc Pelissier	NPTest	President	Universal Instruments	CEO/President
5/1/1997	Jeff Hintzke	Hewlett-Packard	Product Manager	Electroglas	Director of Marketing
2/1/2004	Jeff Hotchkiss	Empirix		Teradyne	
12/1/2002	Jeffrey M. Dumas	Storage Technology	VP, General Counsel	ASAT	Sr. VP, General Counsel
2/1/2006	Jens Meyerhoff	Formfactor	COO	Virage Logic	CFO
7/1/2006	Jens Meyerhoff	VirageLogic	CFO and VP		
9/1/1999	Jerry Broz, Ph.D	Adv. Probing Systems	Director R&D	Texas Instrument	Probe Evaluation Lab
10/1/2002	Jerry Broz, Ph.D	T.I.	Probe Dev. Engineer	Point Technologies	Director of R&D
12/1/2005	Jess DeGennaro	K&S	Sales Position	MCT	VP of Sales
10/1/1999	Jim Anderson	Cerprobe		TSK	
5/1/2005	Jim Bowen	Rockwell	VP	Incal Technology	Board of Directors

7/1/2002	Jim Douglas	Cadence Design		ReShape	CEO
9/1/1998	Jim Healy	Credence Systems		Formfactor	
2/1/2000	Jim Healy	Genus	CEO	FormFactor	VP/GM
5/1/2000	Jim Healy	Formfactor	Executive VP/GM	ASAT	Sr. VP of Worldwide Sales
9/1/2002	Jim Healy			Spirox	VP for Strategic Bus. Dev.
1/1/2004	Jim Healy	Spirox		LogicVision	President/CEO
5/1/1998	Jim Healy	Genus	President		
11/1/2004	Jim Heil	Eagle Test		Advantest	
5/1/1999	Jim Heil	Cohu		TMT	Central Area Sales Mgr
4/1/2005	Jim Reesman	Syntricity	VP software develop.	Logic Vision	Lead Engineer/Architect
5/1/1998	Jim Ward	LTX	Marketing Director	Credence Systems	Director of Strategic Sales
11/1/2006	Joe Kadaras	Asset InteTech		CloverTest Associates	
10/1/2006	Joe Logan	Avant!	Head of N. Am. Sales	Synopsys	Sr. VP
9/1/1998	Joe Rivlin	ESL	Vice President	Veeco Instruments	Executive Vice President
2/1/2005	Joe Serra	Teradyne	Applications Manager	Transcendent Eng.	Founder
7/1/1997	John Arcari	LTX	CFO	Robotic Vision Sys	VP of Finance
5/1/1997	John DeBolt	Siliconix	Program Manager	TYECIN Systems	VP for Engineering
11/1/2001	John J. Connolly	Davox	CFO	Robotic Vision Systems	VP/CFO
4/1/2006	John R. Regazzi	HP/Agilent		Giga-tronics	CEO
3/1/2002	John Schmitz	Philips Semiconductor		Internat Sematech	VP/COO Manufacturing
10/1/1999	Jon D. Tompkins	KLA-Tencor		Credence Systems	Board of Directior
3/1/1998	Jong Beom (J.B.) Kim	Anam Test	Manager of Test Eng.	ChipPac	Manager of Test Dev.
9/1/2008	Jong Ho Yoon	Micro TN		SV Probe	
12/1/2007	Jorge Titinger	KLA-Tencor	Ex. VP of Global Ops.	Formfactor	Sr. VP
7/1/2008	Jorge Titinger	Formfactor	Sr. VP	Verigy	COO
10/1/2007	Joseph Bronson	Applied Materials	Board of Directors	Sanmina-SC	President/CEO
5/1/2007	Joy E. Leo	CoWare	VP of Finance	Credence Systems	VP of Finance
12/1/2006	Judy Davis	Credence Systems	VP of Marketing	Verigy	VP of Investor Relations
4/1/2000	Jue-Hsien Chern	Avant!	head of DSM	Mentor Graphics	VP/GM
3/1/2001	K Y Chan	T.I.'s Unitrode Elect.		STATS	Executive VP
4/1/1998	Karen Lynch	SGS-Thomson		Cerprobe	Dir. of Marketing
5/1/2006	Kathy Werner	Freescale		VSI Alliance (VSIA)	President
2/1/1997	Keith Barnes	IMS	President/CEO	Data I/O	Board of Directors
9/1/2001	Keith Barnes	IMS	Chairman/CEO	Credence Systems	Executive Vice President
11/1/2003	Keith Barnes	Credence Systems	Chairman/CEO of IMS	Electroglas	Chairman/CEO
5/1/2006	Keith Barnes	Electroglas	Chairman/CEO	Verigy	President/CEO
12/1/2002	Keith Jackson	Fairchild Semi	GM of IC Group	On Semiconductor	Presdient/CEO/Director
2/1/2004	Keith Lee	Megatest		Advantest America	President/CEO
3/1/2001	Ken Daub	LTX		Eagle Test Systems	VP of Sales/Marketing
8/1/1998	Ken Gray	Aseco	VP of Sales/Mktg.	Cohu	VP sales/mktg
5/1/1999	Ken Jones	MicroModule Systems		Vitesse Semi	VP of ATE Products
1/1/2007	Ken Karklin	Verigy	Manager Test Cell	Touchdown Tech	VP of Engineering
3/1/2002	Ken Posse	Agilent Tech		Teseda	CTO
8/1/2001	Ken Skala	Kinetix Test System			
11/1/2007	Ken Skala	Credence Systems	Product Marketing	DFT Microsystems	VP of Marketing
4/1/2008	Kenneth Levy	KLA-Tencor	Retired CEO	Optimal Test	Board of Directors
6/1/1999	Kensaku Fujimori	Viewlogic		IKOS KK	President
12/1/1997	Kevin Fetterly	Credence Systems	Marketing Mgr. TSSI	Port Orford Software	Founder
2/1/2008	Kirk Hasserjian	Intel	VP of Flash Memory	Formfactor	Sr. VP of Global Manuf.
11/1/2007	Larry Dibattista	Credence Systems		Verigy	
9/1/2002	Larry Hollatz	AMD	Executive	Numerical Tech.	President/CEO
1/1/2002	Larry Rawstorne	C-Level Design	GM	LogicVision	Business Manager
7/1/1998	Larry Ross	Schlumberger	Director of Sales	TSK	GM of Test and Ass.
8/1/2007	Laura Owen	Credence Systems	VP of Human Resource	Vitria Tech	VP of Human Resource
6/1/2002	Len Perham	IDT	CEO	ASAT	Chairman
4/1/2000	Leo van Bree	Rood Technology	President/CEO	Schlumberger, Europe	VP/GM
7/1/2008	Les Howell	Teradyne	Senior Test Tech	Van Limburg Eng..	Test Engineer

3/1/2004	Lip-Bu Tan	Walden International	Chairman, Founder	Cadence Design Systems	Board of Directors
12/1/2006	Lothar Maler	Linear Tech	CEO	Formfactor	Board of Directors
3/1/2005	Lubab L. Sheet	SemiSales	VP and Co-founder	SEMI	Director of Nanotech
7/1/1998	Mac Makhni	Credence Systems	Account Manager	LTX	
10/1/2002	Marc Corbacho	NetOctave	VP of Sales	Mentor Graphics	VP of Sales
6/1/2007	Maria M. Pope	Pope and Talbot	GM	Mentor Graphics	CFO
2/1/2001	Marius Lupan	TEL America		KLA-Tencor	Sr. Corporate Function
5/1/1998	Mark Goldman	Avant	VP of US Sales	Duet Technologies	Sr. VP of Sales
11/1/2000	Mark J. Gallenberger	Ernst & Young	VP	LTX	VP/CFO
11/1/2005	Mark King	T.I.		Micropac Industries	President and CEO
7/1/2004	Mark Merrill	KLA-Tencor	Chief Marketing Off	Photon Dynamics	VP of Marketing
1/1/2002	Mark Milligan	Synopsys	VP of Marketing	HPL Tech	VP/GM
9/1/2008	Mark Moore	Credence		Teseda	VP of engineering
6/1/2008	Mark Murdza	Antares ATT	Director of Marketing	Cascade Microtech	Sales Manager
7/1/1998	Mark Olen	Mentor Graphics	Head of DFT Group	TSSI	VP of Sales
10/1/2000	Mark Patch	LTX	Global Account Man.	LogicVision	Director of Sales
7/1/2004	Mark Roos	Roos Instruments	CEO	Semi Test Consortium	
10/1/2001	Mark S. Ain	Kronos	Founder and CEO	LTX	Board of Directors
6/1/2005	Maureen L. Lamb	KLA-Tencor	VP of Finance	Photon Dynamics	CFO
6/1/2004	Michael J. Fister	Intel	VP/GM of Platforms	Cadence Desing Sys	President/CEO
3/1/2003	Michael Polcari	IMB	VP Procurement Eng.	Internat. Sematech	CEO
2/1/1997	Michael Sobelman	Schlumberger	Product manager	Credence Systems	Director Memory Test
6/1/2003	Michael Splinter	Intel	Director of Sales	Applied Material	President/CEO
3/1/2001	Michael Wright	Wright Will and Kelley	Founder	Entegris	President
1/1/2004	Michel Villemain	NPTest	VP/GM of Probe	KLA	
2/1/2005	Mike Deal	Credence Systems		Clarity Visual Sys.	VP of Ops.
6/1/1999	Mike Egloff	RSJ Technical Sales		MicroTek Test Eng	Founder
6/1/1998	Mike Epsztein	Schlumberger	VP/GM of ATE	Robotic Vision Systems	President of Automation
8/1/1998	Mike Ferguson	Cadence	VP of Asia-Pacific	Quickturn Design Systems	VP of Asian Operations
6/1/1999	Mike Hackworth	Cirrus Logic	Chairman	Digital Tools Inc.	President/CEO
9/1/2007	Mike Kondrat	Credence Systems	Sr. Director	Cascade Microtech	VP of Marketing
10/1/2004	Mike Purtell	Advantest America	Sr. Product Engineer	National Semi.	Principal Test Engineer
3/1/2004	Mike Seifert	Southwall Tech.	CFO	Virage Logic	CFO
10/1/1997	Miles Prim	Amkor Technology		Amkor Technology	VP of Test Services
1/1/2003	Morris Chang	Goldman Sachs Group	Director	TSMC	Founder/Chairman/CEO
12/1/2002	Motohiko Tahara	Cymer	President	KLA-Tencor	President
9/1/2000	Mukesh Mowji	LTX	VP of Sales	LogicVision	VP of Manufacture Bus
9/1/1999	Mukesh Patel	Smart Modular Tech	Co-founder	Aehr Test Systems	Board of Directors
8/1/2000	Nadim Ahmad	Johnstech		Eagle Test System	West Coast Sales Ops
7/1/2001	Ng Tiong Gee	Gateway Singapore	Chief Information Off.	STATS	Chief Information Officer
9/1/2001	Nicholas Colella	nChip	Co-founder	Tessera	Sr. VP of operations
9/1/2000	Nicholas Konidaris	Advantest America	President/CEO	Ultratech Stepper	Board of Director
2/1/2004	Nick Konidaris	Advantest America	President/CEO	ESI	President/CEO
4/1/2008	Nigel Dessau	IBM		AMD	Chief Marketing Officer
10/1/1999	Oliver C. Davis II	ASAT		Signetics High Tech.	
12/1/2005	P.M. Bijkerk	MSI		Rood Technology	Sales Manager
4/1/2006	Pascal Didier	Megatest	VP of Intern. Ops.	Cymer	President/COO
2/1/2008	Pat Cochran	Freescale Semi	Internal Handler Dev.	Rasco	US Sales Manager
8/1/1997	Pat Reilly	Reid-Ashman Mfg. (RAM)	Director of Sales	Khonectix	VP sales & mkt.
3/1/1998	Patrick Caiger-Smith	Rexam PLC		Western Equip. Dev.	Managing Director
5/1/2007	Patrick J. Brady	Photon Dynamics	VP/GM	Credence Systems	Sr. VP Engineering
12/1/2005	Patrick J. Spratt	KVH Industries	CFO	LTX	Board of Directors
10/1/2002	Patrick McKinney	Amkor Technology	Sr. VP	Entegris	President of Semi Market
10/1/1997	Paul Emmett	Amkor Technology	VP of Test Services	ChipPac	Director of Test Tech
2/1/2004	Paul Emmett	ChipPAC		ASAT	VP of Sales/Services
7/1/2005	Paul Hofstadler	360Bridge	Founder and CEO	Mentor Graphics	VP of Consulting
4/1/2005	Paul J. Tufano	Maxtor	President/CEO/Dir.	Credence Systems	Board of Directors

5/1/1997	Paul Jasmine	Credence Systems		S3	Director of Test Eng.
10/1/2001	Paul Lin	Array Packaging Tech	Founder and Pres.	Kulicke and Soffa	Dir. Process Integration
2/1/2005	Paul Magliocco	Nextest	Founder	Advantest America	Ex. VP
10/1/1997	Paul McLellan	Compass Design Auto	President	Ambit Design Systems	VP of engineering
1/1/2008	Paul Oldham	Tektronix	VP	ESI	CFO
11/1/2005	Paul Roddy	Motorola	Test Tech. Manager	Advantest America	OAI Technical Manager
7/1/2002	Paul Sakamoto	Credence	Executive	Inovys	CEO
5/1/2005	Paul Scriven	LTX	VP of Marketing	LogicVision	Director of marketing
4/1/1998	Paul Scrivens	Credence Systems	Marketing Manager	IMS	G.M.
12/1/1999	Paul Scrivens	IMS	GM of Mixed Signal	SZ Testsystems	President
3/1/1998	Paul Whitman	Electroglas	Sales Manager	TMT	N. CA Sales Manager
7/1/2001	Paul Whitman	Credence		3MTS	N. American Sales Mgr.
10/1/2002	Paul Whitman	3MTS	Director of U.S. Sales	StepTech	VP of Sales
11/1/2004	Peter Hancock	Credence	Oversee SZ Ops	Eagle Test	
5/1/2006	Peter Hancock	Eagle Test	Sales	Best Electronics	COO
6/1/2001	Peter Verhofstadt	Fairchild		Semi Research Corp	Chief Scientist
6/1/2001	Peter Zung	Lam Research		Credence Systems	GM/Director
10/1/1998	Phil Truckly	Electroglas	VP of marketing	Wentworth Labs	
10/1/2004	Philip Nijenhius	Schlumberger	Management	Rood Technology	CEO
6/1/1998	Phill Truckle	Electroglas	VP of Marketing	Wentworth Labs	VP Marketing
6/1/1998	Phillip J. Villari	ESI	GM of chip unit	Aseco	VP of Manufacture
3/1/2006	Rachel Young	Hitachi Data Systems	VP of Marketing	Cadence Design System	VP of Marketing
5/1/2000	Ray Bingham	Cadence Design System	President/CEO	Design Consortium	Chairman
11/1/2000	Ray Bingham	IMS	Chairman		
6/1/2005	Rex S. Jackson	Synopsys	General Council	Synopsys	CFO and General Council
7/1/1999	Ric Dokken	LTX	Apps. Mgr.	New ATE Startup	
10/1/2003	Rich Beyer	Intersil	President/CEO	Credence	Board of Directors
3/1/2008	Rich Beyer	Intersil	CEO	Freescale Semi	CEO
4/1/2000	Rich Davenport	Summit Design's	President/COO		
4/1/2005	Rich Yerganian	LTX	Dir. Investor relations	LTX	Vp of Sales
12/1/1998	Richard Dissly	Megatest	CFO	Photon Dynamics	CFO
10/1/2004	Richard Freeman	ChipPAC	COO	Formfactor	VP of Operations
1/1/2003	Richard H.P. Chang	ASE	Vice-chairman	Aseco	President
4/1/2002	Richard M. Brook	Tanisys Technology	VP		
3/1/2003	Richard Okumoto	TMT	President/CEO	ESI	VP of Admin and CFO
6/1/2003	Richard Okumoto	ESI	CFO	Photon Dynamics	CFO
2/1/2005	Richard Okumoto	Photon Dynamics	CFO	Vitex Systems	Board of Directors
6/1/2007	Richard Okumoto	Photon Dynamics	CFO	LogicVision	Board of Directors
4/1/1998	Richard Okumoto	Credence Systems	Senior VP and CFO		
1/1/2000	Rick Baze	Wavecrest		Alphatech	
7/1/2005	Rick Custance	ESH	Sales and Marketing	Probe 2000	VP of Sales
4/1/1998	Rick Melton	Teradyne		Amkor	G.M. for worldwide test
2/1/2001	Robert Dutkowsky	GenRad		Teradyne	Board Test President
10/1/2006	Robert Dutkowsky	Teradyne	CEO of Genrad	Tech Data	CEO
8/1/2007	Robert H. Therrien	Accutest	Co-founder	Brooks Automation	CEO
10/1/2000	Robert Watson	Signapore Tech Ass Test	Tech Sales Manager	ASAT	Test Sales Manager
3/1/1998	Roel Pieper	Tandem Computers	Executive	Philips elecgtronics	VP of technology strategy
7/1/1998	Roger Bitter	Credence Systems	President/CEO of TSSI	Sycon Design	President/CEO
10/1/2003	Roger Bitter			Tesada	VP of Sales
3/1/2007	Roger Hitchcock	KLA-Tencor		Formfactor	VP
12/1/2000	Roger Hopkins	Aetrium	VP of Sales	Delta Design	Account Mgr.
11/1/1999	Roger Saylor	Teradyne	Mgr. Sales in SE Asia	Teradyne	Sales Manager
12/1/2000	Ron Mende	Probe Technology	CEO	D&S	VP of Marketing
7/1/2004	Ron Mende	K&S	CEO/President	MicroProbe	Executive VP
9/1/2005	Ron Mende	MicroProbe	Executive VP	Probe Technology	President
4/1/2008	Ronal C. Foster	Formfactor	CFO	Micron Tech	CFO/VP of Finance
3/1/2005	Ronald C. Foster	JDS Uniphase	CFO	Formfactor	CFO

9/1/2003	Ronald H. Mabry	PACT XPP Tech	VP of Marketing	LogicVision	VP of Marketing
11/1/2000	Roy Green	ECT		Intest	Interface Dev. Group
3/1/2005	Roy Schmidt	NPTest	VP Fabless Accounts	Pintail Technologies	VP of Worldwide Sales
4/1/2000	Roy Vallee	Avnet	Chairman/CEO	Teradyne	board of directors
2/1/1997	Ruedi Egger	Kulicke & Soffa	Dir. of European Sales	IMS	business mgr.
6/1/1997	Russ Fields	Mosaid	President	CMT	VP of Bus. Dev.
3/1/2006	Russell Schlager	Credence Systems		Cascade Microtech	Dir. of Market and Sales
1/1/2002	Samuel Rubinovitz	LTX	Board of Directors	EG&G	Executive VP
6/1/2006	Sang Park	Hynix		MagnaChip	President/CEO
1/1/2003	Scott Clegg	Cerprobe	Director of R&D	Mergecor	CTO
1/1/2000	Scott Erjavic	Abpac	Dir. of Manufacturing	Artest	VP of Technology
9/1/2004	Scott Jewler	Amkor Technology	Pres. of Taiwan Office	STATS Chip-PAC	
11/1/2004	Scott McGregor	Philips Semiconductor	President/CEO	Broadcom	President/CEO
7/1/1998	Sebastian Sicari	Aseco	CFO	Aseco	President/COO
6/1/2004	Selina Gonzales	K&S		DCI	Sales Manager
10/1/1998	Sergio Perez	Teradyne/Megatest	Marketing Manager	Comdisco Electronics	Director of ATE Tech
4/1/2002	Sergio Perez	Comdisco	VP Bus. Dev.	Advantest America	VP of Sales
4/1/2008	Sergio Perez	Formfactor		SV Probe	Sr. VP
1/1/2000	Shane Robinson	Cadence Design	President of Design	AT&T Labs	Head of Internet Tech.
9/1/2008	Sherry Garber	Semico Research		Convergent Semi	
10/1/1997	Shoichi Hori	Apple Computer	Dir. of Japan Business	Viewlogic Systems	VP of Japan operations
9/1/2006	Stan Semuskie	Credence Systems	Service position	Eagle Test	VP of Customer Service
6/1/2002	Steve Chen	Schlumberger	Sales and Marketing	Credence Systems	GM
6/1/2006	Steve Dale	Aetrium		InTEST	Regional Sales Manager
11/1/2005	Steve Lilly	3MTS	Director of Sales	Incal Technology	US Sales Manager
11/1/2000	Steve Radakovich	ESH	COO	Intest	
6/1/1998	Steve Weisbrod	MCT		Aetrium	VP of Technology
9/1/1997	Steven Chan	Schlumberger		ECTS	VP of Marketing and Sales
1/1/2002	Steven DiCampo	PRI Automation	Manager of Cost	ThetaDelta Tech	Dir. Of Engineering
6/1/2005	Steven K. Shevick	Synopsys	CFO	Wyse Technology	CFO
5/1/2005	Steven Tsuh	Agilent/HP	Marketing Mgr. Asia	Incal Technology	Director of Asia Sales
1/1/2008	Steven W. Berglund	Trimble Navigation	President/CEO	Verigy	Board of Directors
8/1/2000	Sung-Ki Suh	A-Tech	President	SEMI	Chairman
3/1/2006	Surinder Bedi	Applied Materials	VP of Global Quality	Formfactor	VP of Quality
10/1/2006	Tammy Lee McClure	GuideTech	VP Marketing	Solaria	Director of Marketing
10/1/2003	Tammy Pelissier	GuideTech	VP	Altera	Dir. of Test and Medical
1/1/2001	Thomas E. Brunton	Centigram Comm	CFO	Electroglas	CFO
9/1/2003	Thomas J. Campbell	UC Berkeley	Dean of Haas School	Formfactor	Director
6/1/2005	Thomas J.Reilly	Arthur anderson	Audit Partner	inTEST	Board of Directors
10/1/1997	Tim Goswell	Alphatec		Amkor Technology	Director of Marketing
12/1/2000	Tim Olson	Infinity Systems		MCT	Ex. VP of Ops.
4/1/2000	Timothy O'Donnell	ARM Inc.	founder/president	VSIA	VP
2/1/2001	Todd Del Vecchio	Agilent Technologies		Credence Systems	Director of Bus. Dev.
11/1/2003	Tom Anderson	Guidetech		Wavecrest	Sr. Product Apps. Eng.
7/1/1999	Tom Beckley	Xynetix	President/CEO	Avant	Executive staff of Finance
7/1/2007	Tom Gerst	ATFab		JMC	
7/1/2008	Tom Goodnow	LTX		Johnstech	VP of Sales
12/1/1997	Tom Mordue	Credence		LTX	Account Mgr.
1/1/2000	Tom Mordue	LTX		Comdisco Electronics	Manager of Sales
10/1/2000	Tom Mordue	Comdisco		ASAT	
5/1/2003	Tom Mordue	Eagle Test Systems		Wavecrest	Sales Force
11/1/2003	Tom Mordue	WaveCrest	Dir. of N. Amer. Sales		
2/1/2006	Tom Wu	KLA-Tencor	VP of China Ops.	ESI	VP
6/1/2008	Tom Wu	Electro Scientific Indust	VP of Sales	ASM International	VP of Sales
2/1/2000	Tommie Berry	LTX	VP	Inovys	
1/1/2008	Toshi Yamanouchi	Agilent Tech	Country Mgr. Japan	Credence Systems	County Manager
7/1/2005	Toshio Natuyama	Advantest	President/COO	Advantest	CEO/President

2/1/2000	Vic Kulkarni	Avant!		Frequency Technology	VP of mktg.
8/1/2000	Vic Kulkarni	Avant!, VLSI, National SEM	VP of Mktg.	Sequence Design	COO
9/1/2000	Vincent F. Sollitto	Photon Dynamics	President/CEO	Ultratech Stepper	Board of Director
12/1/1997	Vincent M. DePalma	IBM	VP	Photon Dynamics	VP of Technology
11/1/2001	Walter Prochaska	Chartered Semi		STATS	VP for Europe
1/1/2007	Wendell T. Blonigan	Applied Materials	President of AKT	Photon Dynamics	VP/COO
1/1/1998	William Haydamack	Data I/O	Sr. VP	Electroglas	VP
11/1/2002	Willy Yang	Sigurd Microelectronics	Dir. of Operations	Multitest	Head of Sales in Taiwan
9/1/2000	Wim Roelandts	Xilinx	President/CEO	The fabless Semi Assoc	Chairman
11/1/1997	Wolfram Blume	MicroSim	Chairman/Pres./CEO	OrCAD	Chief Technology Officer
5/1/2001	Yoshikazu Hatsukano	Hitachi Microsystems	President	Formfactor	President in Asia
2/1/2008	Yoshio Nakamura	UltraTech	President	Electro Scientific	Board of Directors
8/1/2001	Yoshio Yamanaka	Teradyne KK		Jem Japan	regional sales manager

EXHIBIT 7

News Release

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LTX and Credence Complete Merger to Form LTX-Credence

New Combined Company Provides Focused, Cost-Optimized ATE Solutions for the Wireless, Computing, Automotive, and Entertainment Markets

MILPITAS, Calif., Aug. 29, 2008 (GLOBE NEWSWIRE) -- LTX Corporation (NasdaqGM:LTXX - News) and Credence Systems Corporation (NasdaqGM:CMOS - News) today announced the completion of their merger, resulting in the formation of LTX-Credence Corporation, a global provider of focused, cost-optimized ATE solutions. The companies combined earlier today in a tax free, all-stock merger of equals following the approval of both companies' stockholders yesterday. Beginning Tuesday, September 2, 2008, LTX-Credence, headquartered in Milpitas, California, will trade on the NASDAQ Global Market under the new symbol ``LTXC.''

Under the terms of the merger agreement, Credence stockholders received 0.6129 shares of LTX-Credence common stock for each share of Credence common stock they own, causing the former stockholders of Credence to hold 50.02% of the outstanding shares of the combined company and pre-merger LTX stockholders to hold 49.98% of the outstanding shares of the combined company. As of today's market close, shares of Credence common stock will cease trading on the NASDAQ Global Market.

``I am excited to announce the completion of the merger of LTX and Credence, and I am confident that the combined strengths of the two companies will create a leading provider of focused, cost-optimized ATE solutions,'' noted Dave Tacelli, chief executive officer and president of LTX-Credence. ``We have worked diligently to close this transaction, and have successfully completed the merger ahead of schedule. Now, with our seasoned leadership team in place, we will push forward with that same intensity as we move through the integration process and drive to rapidly deliver the advantages of the new LTX-Credence to our stockholders, our customers and our employees.''

Tacelli continued, ``We see significant advantages for all LTX-Credence stakeholders. We believe that the combined company's financial strength, operational efficiency and growth opportunities will allow us to deliver superior value to our stockholders. Our customers will benefit from our broad portfolio of technologies, the largest installed base in the Asia-Pacific region, and an unmatched global network of applications and support resources. The infusion of fresh ideas and approaches across our combined employee base will not only enhance the solutions we develop for our customers, but also greatly expand opportunities for growth and leadership for our employees.''

LTX-Credence will provide an update on the progress of the company's integration activities during a conference call the first full week of October 2008. Additional details regarding the conference call will be provided as they become available.

About LTX-Credence Corporation

Formed by the 2008 merger of LTX Corporation and Credence Systems Corporation, LTX-Credence is a global provider of focused, cost-optimized ATE solutions designed to enable customers to implement best-in-class test strategies to maximize their profitability. LTX-Credence addresses the broad, divergent test requirements of the wireless, computing, automotive and entertainment market segments, offering a comprehensive portfolio of technologies, the largest installed base in the Asia-Pacific region, and a global network of strategically deployed applications and support resources. Additional information can be found at http://www.LTX-Credence.com.

Safe Harbor for Forward-looking Statements

Statements in this press release regarding the transaction between LTX and Credence, including the belief that the combined strengths of the two companies will create a global provider of focused, cost-optimized ATE solutions, the tax-free nature of the transaction, the belief that LTX-Credence can move through the integration process and drive to rapidly deliver the advantages of LTX-Credence to its stockholders, its customers and its employees, the belief that the merger will result in significant advantages for all LTX-Credence stakeholders, the belief that LTX-Credence's financial strength, operational efficiency and growth opportunities will allow it to deliver superior value to its stockholders, the belief that LTX-Credence's customers will benefit from its broad portfolio of technologies, applications and support resources, and the belief that the merger will result in an infusion of fresh ideas and approaches across the LTX-Credence employee base that will enhance the solutions LTX-Credence develops for its customers and greatly expand opportunities for growth and leadership for its employees, and any other statements about LTX-Credence management's future expectations, beliefs, goals, plans or prospects constitute forward-looking statements within the meaning of the Private Securities Litigation Reform Act of 1995. Any statements that are not statements of historical fact (including statements containing ``believes,'' ``anticipates,'' ``plans,'' ``expects,'' ``may,'' ``will,'' ``would,'' ``intends,'' ``estimates''

Stock Quote

LTXX (Common Stock)

Exchange	NASDAQ GM (US Dollar)
Price	$1.79
Change (%)	0.00 (8.67%)
Volume	0

Data as of 08/29/08 4:00 p.m. ET
Minimum 20 minute delay
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and similar expressions) should also be considered to be forward-looking statements. There are a number of important factors that could cause actual results or events to differ materially from those indicated by such forward-looking statements, including: the ability to successfully integrate LTX's and Credence's operations and employees; the ability to realize anticipated synergies and cost savings; the risk of fluctuations in sales and operating results; risks related to the timely development of new products, options and software applications and the other factors described in LTX's Annual Report on Form 10-K for the fiscal year ended July 31, 2007, Credence's Annual Report on Form 10-K for the fiscal year ended November 3, 2007, their most recent Quarterly Reports on Form 10-Q and their joint proxy statement/prospectus dated July 29, 2008, each as filed with the SEC. LTX-Credence disclaims any intention or obligation to update any forward-looking statements as a result of developments occurring after the date of this press release.

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www.ltx-credence.com

Source: LTX-Credence Corporation